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3. C4600 Transformer Secondary Circuit Breakers

6.1.1 Release of FMI-108 for SP1000/CD's

A possible problem was discovered on older CD's that the AC power filter cover may cause a short between the filter cover and the filter studs. A new cover has been released and needs to be installed on any effected CD's.

If you received a CD shipped this Summer or early Fall, you need to visually inspect the filter cover to see if it is the one in question. The suspect filter cover is P/N 325-000050-500 and has a small step at the power supply end of the cover. Some CD's shipped during this period and into the Fall were shipped with a cover that did not have a step, 325-000050-500 Rev A, they are not to be changed. The replacement cover is P/N 325-000050-501.

To visually inspect the cover you can either remove one of the cable plates on the back of CD and with a flashlight, look down into CD to check or you can remove the system cover and then inspect it. Once you have identified that you have the suspect filter cover, you need to contact Convex Logistics for the replacement.

6.1.2 SPP Component Locations

The cst utility will generate failures using fixed location coordinates, to report a component failure. An example of this is shown below:

```
Wire XQMC1PAR0  (ring 0 -> ring 3)
Driver:   XBAR Z073K8.AP39                    ODP1_0 bit -255 Hi
Recver:  CCMC2 Z131F5.J6            XB_CM_RQI_DPAR_0 bit  415 Lo
Pattern 0008 - ac_pat.008 FAILED  1 error
```

From this information, it is difficult to know which CCMC, or Xbar is involved, from the location Z073K8. To aid in the identification, the location can be determined by a couple of simple methods.

First of all the slice is indicated by the last two digits. These will be as follow:

slice 0 is C0
slice 1 is F5
slice 2 is P4
slice 3 is T9

The XBQ, XBS and Maui are located at K8.

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6.1.2 SPP Component Locations (continued)

The first 4 digits indicate the actual component, as follow:

Agent is Z058
CCMC is Z131
SCI is Z163
XBQ is Z073
XBS is Z102
Maui is Z131

So, from this it is possible to determine, from the info, in the error, that the failing CCMC is in slice 1 and the Xbar device is the XBQ, or xbar request gate array.

6.1.3 C4600 Transformer Secondary Circuit Breakers

This is intended for informational use only.

Maximum breaker sizes are:
60 amps/phase for Saturn I/O
80 amps/phase for Saturn CPU.

Theses sizes are based on maximum allowed service due to power sizing of Saturn primary components. These components were sized based on early Saturn maximum estimates.

WARNING It is always recommended that the maximum breaker size be installed, even on smaller systems. This will prevent power problems from interfering with upgrades.

MINIMUM BREAKER SIZES

Now that systems have been characterized there are minimum values for breakers which are more inline with actual current values. These values still include sufficient pad (at least 25%) to prevent nuisance tripping.

Saturn I/O 30A

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6.1.3 C4600 Transformer Secondary Circuit Breakers (continued)

Saturn CPU Config	Amps/ph @Low Line & Margin	Minimum Breaker Size	Nearest Domestic Breaker Size

1	SPR/1SMB	11.2	14.0	15
1	SPR/2SMB	17.1	21.4	25
1	SPR/4SMB	28.9	36.2	40
2	SPR/1SMB	15.7	19.7	20
2	SPR/2SMB	20.8	26.0	30
2	SPR/4SMB	32.6	40.8	45
3	SPR/1SMB	20.2	25.3	30
3	SPR/2SMB	25.3	31.7	35
3	SPR/4SMB	36.3	45.4	50
4	SPR/1SMB	24.8	31.0	35
4	SPR/2SMB	29.8	37.3	40
4	SPR/4SMB	40.0	50.0	50

BREAKER CHARACTERISTICS

Minimum voltage rating - 250VAC RMS Minimum
Interrupt Capacity - 5000 Amperes at 50/60Hz
Trip Delay -

100% Rating	- No Trip		
125% Rating	- 12	- 100	Seconds
150% Rating	- 6	- 50	Seconds
200% Rating	- 2	- 18	Seconds
400% Rating	- 0.3	- 3	Seconds
600% Rating	- 0.05	- 2	Seconds
800% Rating	- 0.016	- 1.6	Seconds
1000% Rating	- 0.01	- 1	Seconds

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1. New SPP Related FMI's
2. SPP1000/CD Disk Address Jumpers
3. C4600 Connectivity Testing

6.2.1 New SPP Related FMI's

FMI 105 and 106 have now been released, for SPP systems.

FM0105 exists to verify that specific etches, associated with SCI have been cut on the CSB. These etches involve a timing delay used on the SCI rings and therefore is fairly important when trying to run in a multinode configuration.

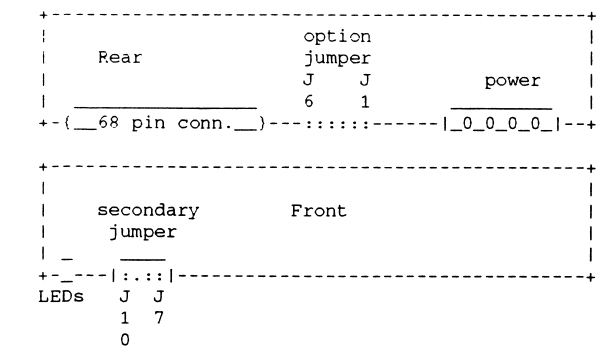
FM0106 is to insure that the MU labels have been changed after the 2.0 firmware upgrade.

Neither FMI involves all systems, so the effectivity list, on the FMI, require review, before proceeding.

6.2.2 SPP1000/CD Disk Address Jumpers

Disk Drive Jumpers DEC DSP3210W 2 GB SCSI 204-000028-200

The unit select jumpers have to be set on the disk for a CD I/O chassis. Unit selection is assigned by chassis slot in the XA I/O chassis. The following gives jumper locations, their meanings and default settings.



Since this device is SCSI wide (i.e. can support SCSI ID 0x0 through 0xF), four (4) jumpers are required to set the SCSI id.

6.2.2 SPP1000/CD Disk Address Jumpers (continued)

Jumper	Setting	Description
J6	Out	(Normal Setting) No Remote LED
	In	Remote LED -- Refer to Digital Instruction Manual
J5	Out	(Normal Setting) Active Termination Disabled
	In	Active Termination enabled
J4	Out	SCSI ID bit3 (MSB) = 0
	In	SCSI ID bit3 = 1
J3	Out	SCSI ID bit2 = 0
	In	SCSI ID bit2 = 1
J2	Out	SCSI ID bit1 = 0
	In	SCSI ID bit1 = 1
J1	Out	SCSI ID bit0 (LSB) = 0
	In	SCSI ID bit0 = 1
J7	Out	(Normal Setting) Write Protect Disabled
	In	Write Protect Enabled
J8	Out	(Normal Setting) Spindle Sync disabled
	In	Spindle Sync Input
J9	Out	Single Jumper (key), not used
J10	In	(Normal Setting) Spin up on power-on
	Out	Don't spin up on power-on
J11	In	(Normal Setting) Supply Term Power
	Out	Don't supply Term Power to SCSI bus

6.2.3 C4600 Connectivity Testing

The C4600 connectivity is tested by means of sss (sst), rather the spu4000, subtest 810, utilized by the 3800. Because of this, the process of data collection and identification is somewhat different.

The first obstacle involves proper setup of sss, so that the failure is given in some way that makes sense. To accomplish that is very similar to execution of sst, with a couple of differences.

There are two test parameter menus involved. The first menu is the test limit menu, which can be reached through the test parameter menu.

6.2.3 C4600 Connectivity Testing (continued)

To get the proper display, the folowing menu entries should be enabled:

```
   3 eliminate failure sources
  10 enable second source NFS data acquisition
  11 enable connection patterns
```

All other entries should be off.

After the test is set up correctly, it is necessary to adjust the display parameters, in the display parameter menu. The entry is the failure menu, which can be entered by a 3 at the prompt. To set the display, simply enable the following:

```
   3  display identified failing networks
   4  display connector pin info every failure
   5  display updated best guess every failure
```

After these parameters have been entered, it is then possible to interpret the failure date. The failures will be reported in the form:

```
 ------------- Failure Isolation Data -------------
  SOURCE  SOURCE                SOURCE              SOURCE          SRC
  BOARD   SCAN BIT              SIGNAL NAME         CONNECTOR PIN   VAL
  DEST    DESTINATION           DESTINATION         DESTINATION     DEST
  BOARD   SCAN BIT              SIGNAL NAME         CONNECTOR PIN   VAL

stuck-at fault:
  xb      xr.xb_m4_data_1<16>   XB_M4.DATA<48>      Z188V3-G17      0
  cu      l1_wr_edat<16>        XSE_CU.WR_DATA<16>  Z220T7-4_206    1
```

The SOURCE CONNECTOR PIN and DESTINATION CONNECTOR PIN are reported in a coordinate format. The first character indicates the side of the backplane that the connector is located on. For the CPU bay, the Z side is the side with the odd processors and memory installed.

The next 3 digits indicate the location of the component along the horizontal length of the backplane. THe last two characters give the vertical coordinates along the backplane. After the hyphen, is indicated the exact segment and pin location. For the example above Z188V3-G17 indicates that this location is on the Z side, to the far side of the backplane (188) and is nearer to the bottom (V3). The G17 is the pin coordinate.

6.2.3 C4600 Connectivity Testing (continued)

In the case of Z188, this is the horzontal location of the flex connectors. These connectors can be identified, as follows:

```
   E3   J25
   K3   J26
   P3   J27
   V3   J28
```

Most other connectors can be located by the signal name, similar to the 3800.

For the other location, Z220T7-4_206, the signal identifies it as a CU slot and the 4_206 indicates segment 4, pin 206.

Using these rules, there should be no problem locating a specific net.

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2. SPP1000 - Disabling Nodes and Slices when Trouble-Shooting
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4. TOC sync Errors on SPP
5. C4600 io5000.t Diag Failure
6. CXTS for C4600's

6.3.1 SPP1000 - Saving Parameters Before Trouble-Shooting

There are 2 teststation commands that allow you to save and restore node parameters before and after trouble-shooting a SPP1000.

The "saveall" command will save all of the MU's NVRAM for a particular node. This includes mu_fw, pl and OBP.

```
saveall <node#> /spp/firmware/<filename<node#>>
```

You must execute the "saveall" command for each node.

The "restall" command will restore all of the MU's NVRAM for a particular node.

```
restall <node#> /spp/firmware/<filename<node#>>
```

It is recommended to "saveall" after each mu_fw, pl and OBP upgrade or permanent parameter change. Additionally you should "saveall" before trouble-shooting problems.

6.3.2 SPP1000 - Disabling Nodes and Slices when Trouble-Shooting

When trouble shooting SPP100's it is sometimes necessary to disable a node or slice to locate the problem.

To disable a slice, use xconfig and de-select the particular slice in each node. Do a download. Do a do_reset 3. Continue trouble-shooting. After the problem has been resolved, use ccmu to restore the original parameters.

```
ccmu> pull
ccmu> quit
do_reset 3
```

To disable a node, use ccmu.

```
ccmu> up
ccmu> select
ccmu> clear <node#> n
ccmu> auto
ccmu> down
ccmu> quit
```

Do a do_reset 3. Continue trouble-shooting.

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6.3.2 SPP1000 - Disabling Nodes and Slices when Trouble-Shooting (continued)

After the problem has been resolved, use ccmu to restore the original parameters.

```
ccmu> pull
ccmu> quit
do_reset 3
```

6.3.3 Release of FMI-107 for 2-4 node SPP1000/XA's

Title:
SCI Collision Avoidance Modules in 2-4 node SPP1000s with GSM gate arrays.

Purpose:
Correct RESP_RQ_ERRs and SCI CRC errors when running GSM applications.

Priority:
Must be installed in 2-4 node SPP1000s, with SCI2 rev B and CCMC2 rev B gate arrays, before running SPP-UX 3.0 or higher.

6.3.4 TOC sync Errors on SPP

The following errors can be expected to accompany failures, on SPP multi node systems:

```
[72000001 001df2ec 1:5] Node 1, CPU 5 detected loss of TOC sync.
[72000001 001df2ec 2:5] Node 2, CPU 5 detected loss of TOC sync.
[72000001 001df2ec 3:5] Node 3, CPU 5 detected loss of TOC sync.
```

This occurs in response to hard_logger stopping clocks on one node. All other nodes will respond with a loss of "TOC sync". This error should be ignored, unless it occurs with no other errors present.

One helpful hint may be that the error appears to occur on all nodes except the one that had the original failure.

6.3.5 C4600 io5000.t Diag Failure

Diagnostic io5000.t will fail subtest 230, on 50Hz systems. This test is a line-frequency test and will fail due to 500 interrupts being handled in 8 seconds, as opposed to the expected 9-11 seconds.

It is suspected that the difference in Pbus timing, between the C4600 and C3800 may be the culprit, but it is not known for sure.

6.3.6 CXTS for C4600's

V1.5 CXTS is released and can be used on the C4. This release supports, primarily, automatic VIPER updating and FE, or TAC notification, of specific failures.

This software will respond to more than 60 different system events. These events cover just about any unexpected system failure, or problem.

This software does not cost CONVEX anything, as licenses were purchased in advance. The only thing required is an internet connection, for the SPU.

When installed, a directory, cxts, will be created under /diag. This directory will include a separate path for cobra and for notification.

The automatic VIPER updates can be enabled by copying the file /diag/cxts/cobra/COBRA_crontab to /users/diaguser/.crontab and executing cron -e /users/diaguser/.crontab. After this, setup the notification.setup to repond to the event, EC_MAIL_CXTS_REPORT. The full entry, in the notification.setup would appear as:

```
{
#  comment
    event_type      EC_MAIL_CXTS_REPORT
    threshold_type  MAX
    count           1
    timeframe       1
    [
    mail_to      cxts_reports
    mail_from    SPU
    system       cat /diag/cxts/reports/mail_report >>
                  /diag/cxts/notification/message
    system       rm /diag/cxts/reports/mail_report
    ]
}
```

A notification browser exists, for the notification function. To set up notification, it is only necessary to create a notification.setup file, under /diag/cxts/notification, using the notification browser. This will allow the selection of system events, to respond to, alias and path of individuals to notify and special responses, shuch as sending the errlog.

It is even possible to set up a system event that would page the FE, for specific problems.

Recommended events to take action on, are as follows:

```
EC_APR_DONE
EC_MAIL_CXTS_REPORT
EC_CONFIG_ERR
EC_HARD_ERR
EC_HARDLOG_END
EC_SOFT_ERR
EC_ENV_ERR
EC_OS_HANG
EC_EGOS_PANIC
EC_OS_REBOOT
```


6.3.6 CXTS for C4600's (continued)

The notification.setup can even be edited and created directly, if use of the browser is undesirable. A sample file would be as follows:

```
{
# comment
   event_type EC_MAIL_CXTS_REPORT
   threshold_type MAX
   count 1
   timeframe 1
   [
   mail_to haddix@convex.com
   mail_from SPU
   system cat /diag/cxts/reports/mail_report >>    ## Should be on one
                                                      line
              /diag/cxts/notification/message
               system rm /diag/cxts/reports/mail_report

   ]
}

{
# comment
   event_type EC_CONFIG_ERR
   threshold_type MAX
   count 1
   timeframe 1
   [
   mail_to haddix@convex.com
   mail_from SPU
   ]
}

{
# comment
   event_type EC_HARDLOG_END
   threshold_type MAX
   count 1
   timeframe 1
   [
   mail_to haddix@convex.com
   mail_from SPU
   system  tail -200 /mnt/errlog > /diag/cxts/notification/message
   ]
}
```

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2. METRUM RSP-2150 Error Codes
3. SPP1000 2.1 mu_fw Breaks MOD Light Programs
4. C4600 Memory Failure Analysis

6.4.1 METRUM RSP-2150 Drives

All new drives purchased from Metrum, from now on, will contain a differential interface.

If you are purchasing drives for a new customer, or adding drives to an existing customer site, please note this fact. It should also be understood by all that this change now makes it mandatory to use a different SCSI controller, Interface cables, and Drive terminators.

Both types of drives will be available to allow us to service the installed base that we have, and the can be ordered by using the following part numbers:-

TAPE DRIVE, RSP-2150, METRUM SE SCSI 207-000023-201
TERMINATOR, RSP-2150, METRUM Single-Ended SCSI interface ..207-002150-001

TAPE DRIVE, RSP-2150, METRUM, Differential 207-000025-201
TERMINATOR, RSP-2150, METRUM, Differential 207-000015-011

6.4.2 METRUM RSP-2150 Error Codes

The following is provided for informational purposes only. It is not intended to be used to trouble-shoot a Metrum drive to a failing PCB or mechanical component. Attempts to fix a unit at this level in the field may void the warranty.

RSP-2150 ERROR MESSAGES

GENERAL

Table A-1 lists the error messages that can be displayed on the RSP-2150 front panel. See the appropriate host computer manual for a complete list of system error messages.

When an error is encountered:

1. Record error message(s).
2. Cycle power to OFF then ON.
3. Repeat process that caused error to be generated. If the identical error message(s) are re-displayed, contact the distributor or service representative.

6.4.2 METRUM RSP-2150 Error Codes (continued)

Table A-1. Front Panel Error Messages

Error	Message	Description
001	Bus error	CPU Bus error condition detect.
002	ADDS error	CPU Address error condition detect.
003	Illegal INST	CPU Illegal Instruction condition detect.
004	Zero Divide	CPU zero divide condition detect.
005	CHK INST	CPU Check Instruction condition detect.
006	Trap error	CPU Unused trap detect.
007	Privilege EB	CPU Privilege violation detect.
008	Trace error	CPU Trace error detect.
009	101 Error	CPU 101 Instruction detect.
010	111 Error	CPU 111 Instruction detect.
011	UIV Error	CPU UIV Interrupt detect.
012	Undefine INT	CPU Unused interrupt detect.
013	TTP Failure	TTP Command register verity error.
014	DC +5V Down	TTP Power +5V fail.
015	Mecha error	Unrecoverable error detected in TTP.
018	Drive error	Unrecoverable error detected in drive control.
017	DMA UnderRUN	Data transfer DMA did not terminate within master SYNC.
018	No Data RAM	Buffer manager data RAM Is absent or failed.

(1) Start up Problems

PROBLEMS	PROCEDURE
Doesn't Power ON	1. Check fuses and voltage selector. 2. Replace Power Supply.
LCD display is off	1. Check DIP switches on BUFFER MANAGER card. 2. Replace BUFFER MANAGER card.
Defective LCD display	1. Replace OPERATION card. 2. Replace BUFFER MANAGER card.
Hang up on Initializing	1. Check DIP switches on DRIVE CONTROLLER card. 2. Replace DRIVE CONTROLLER card. 3. Replace BUFFER MANAGER card.
Can't operate front KEYS	1. Replace BUFFER MANAGER card. 2. Replace PERSONALITY card.
LCD flashing SYSTEM Error	If SYSTEM Error (BF), see pages 4 & 5 of this bulletin.

If SYSTEM Error (DR), see page 6 of this bulletin.

6.4.2 METRUM RSP-2150 Error Codes (continued)

(2) Insert a TAPE

PROBLEMS	PROCEDURE
Format testing doesn't work.	1. Replace DATA CH (ENC) card. 2. Replace DRIVE CONTROLLER card. 3. Replace BUFFER MANAGER card.
Hang up on Format testing.	1. Check DIP switch on TTP card. 2. Replace DRIVE CONTROLLER card. 3. Replace TTP card.
LCD flashing SYSTEM error.	If SYSTEM Error (BF), see pages 4 & 5 of this bulletin. If SYSTEM Error (DR), see page 6 of this bulletin.

(3) During Operation

PROBLEMS	PROCEDURE
Check Condition 03 MEDIUM ERROR on SCSI status	1. Change TAPE cartridge. 2. Clean HEADS (see maintenance procedures). 3. DATA CHANNEL (ENC) DATA CHANNEL (DEC) Replace first circuit card, then if problem still occurs, reinstall the original and replace the next. 4. Adjust BIT SYNCHRONIZER card. 5. Replace BIT SYNCHRONIZER card and calibrate. 6. Replace TRANSPORT Assembly and calibrate BIT SYNCHRONIZER.
LCD flashing SYSTEM ERROR	If SYSTEM Error (BF), see pages 4 & 5 of this bulletin. If SYSTEM Error (DR), see page 6 of this bulletin.

6.4.2 METRUM RSP-2150 Error Codes (continued)

Error code as shown on front panel LCD

SYSTEM Error (BF)
CCC mmmmmmmmmmm

Error Code	PROCEDURE
001 Bus Error	1. Replace DRIVE CONTROLLER card. 2. Replace PERSONALITY card. 3. Replace BUFFER MANAGER card.
002 ADDR Error	1. Replace BUFFER MANAGER card.
003 ILLegal INST	
004 Zero Divide	
003 CHK INST	
006 Trap Error	
007 Privilege ER	
008 Trace Error	
009 101 Error	
010 111 Error	
011 UIV Error	
012 Undefine INT	
013 TTP Failure	1. Replace DRIVE CONTROLLER card. 2. Replace TRANSPORT Assembly and calibrate BIT SYNCHRONIZER.
014 DC +5V Down	1. Check +5 volts at power supply. 2. Replace POWER SUPPLY assembly.
015 Mecha error	1. Replace TRANSPORT Assembly and calibrate BIT SYNCHRONIZER. 2. Replace DRIVE CONTROLLER card. 3. Replace BUFFER MANAGER card.
016 Drive error	1. Repace DRIVE CONTROLLER card.
017 DMA UnderRun	
018 No Data RAM	1. Repace BUFFER MANAGER card.
019 System error	
020 No PSNLTY	1. Replace PERSONALITY card.
021 PSNLTY ID_ER	2. Replace BUFFER MANAGER card.
022 Drive T Out	
023 Dew Detect	
024-029 Not used	

6.4.2 METRUM RSP-2150 Error Codes (continued)

Error code	PROCEDURE
030 BE CPU P ERR	1. Check DIP switch on BUFFER MANAGER card. 2. Replace BUFFER MANAGER card.
031 DMAO P Error	1. Replace BUFFER MANAGER card.
032 DMAO Config	2. Replace PERSONALITY card.
033 DMAO Timing	
034 DMAO Undef	
035 DMAO EXT STP	
036 DMAO SFT ABT	
037 DMAO CNT ERR	
038 DMAO ADR ERR	
039 DMAO BUS ERR	
040 DR DMA P ERR	1. Repace BUFFER MANAGER card.
041 DMA1 P-Error	2. Replace DRIVE CONTROLLER card.
042 DMA1 Config	
043 DMA1 Timing	
044 DMA1 Undef	
045 DMA1 EXT STP	
046 DMA1 SFT ABT	
047 DMA1 CNT ERR	
048 DMA1 ADR ERR	
049 DMA1 BUS ERR	
050 Not Used	
051 SPC TC PERR	1. Replace PERSONALITY card.
052 SPC PH ERR	1. Replace BUFFER MANAGER card.
053 SPC TRS PRIE	
054 SPC TRS OFFE	
055 SPC Error	
056 Not used	
057 RESET Failure	1. Replace DRIVE CONTROLLER card. 2. Replace BUFFER MANAGER card, 3. Replace TRANSPORT Assembly and calibrate BIT SYNCHRONIZER.
058 SPC Time Out	Not Used.
059 SPC TRS BUSY	1. Replace BUFFER MANAGER card. 2. Replace PERSONALITY card.

6.4.2 METRUM RSP-2150 Error Codes (continued)

Error code as shown on front panel LCD — SYSTEM Error (DR)
ccc mmmmmmmmmmmm

Error code	PROCEDURE
030 DR CPU P ERR	1. Check DIP switches on DRIVE CONTROLLER CARD. 2. Replace DRIVE CONTROLLER card.
031 DMAO P Error	1. Replace DRIVE CONTROLLER card.
032 DMAO Config	2. Replace BUFFER MANAGER card.
033 DMAO Timing	
034 DMAO Undef	
035 DMAO EXT STP	
036 DMAO SFT ABT	
037 DMAO CNT ERR	
038 DMAO ADR ERR	
039 DMAO BUS ERR	
041 DMA1 P-Error	1. Replace DRIVE CONTROLLER card.
042 DMA1 Config	2. Replace DATA CH (ENC) card.
043 DMA1 Timing	3. Replace DATA CH (DEC) card.
044 DMA1 Undef	
045 DMA1 EXT STP	
046 DMA1 SFT ABT	
047 DMA1 CNT ERR	
048 DMA1 ADR ERR	
049 DMA1 BUS ERR	

6.4.2 METRUM RSP-2150 Error Codes (continued)

SYSTEM ERRORS AS SEEN ON FRONT PANEL LCD — SYSTEM ER-xxyyzz
015 Mecha Error

xx	BIT	POSSIBLE CAUSES
	7: CYLINDER MOTOR ERROR	CYLINDER MOTOR or SERVO BOARD
	6: CAPSTAN MOTOR ERROR	CAPSTAN MOTOR or SERVO BOARD
	5: REEL ROTATION ERROR	REEL MOTOR or RMJC BOARD
	4: LOADING MOTOR ERROR	LOADING MOTOR or TTP BOARD
	3: TAPE LOADING ERROR	LOADING MOTOR or TTP BOARD
	2: EOM/BOM LEAD FAIL	EOM/BOM SENSER or TTP BOARD
	1: SOLENOID FAIL	BRADE SOLENOID or TTP BOARD
	0: DEW	
yy		
	7: LOW VOLTAGE	
	6: FULL ERASE ERROR	FULL ERASE HEAD or TTP BOARD
	5: CTL REC ERROR	CTL HEAD or SERVO BOARD
	4: LOW ATF RF LEVEL	SERVO BOARD
	3: F2 DETECT ERROR	SERVO BOARD
	2: TENSION SERVO ERROR	REEL MOTOR or SERVO BOARD

```
       1: TRACKING ERROR              SERVO BOARD
       0: SERVO IF ERROR              SERVO or TTP BOARD

zz
       7: RESERVED
       6: DRIVE ERROR
       5: EOM (End of Media)
       4: BOM (Beginning of Media)
       3: CTL (No control pulses)
       2: EM (End Mark - not currently implemented)
       1: VN (volume number)
       0: FM (File Mark)
```

6.4.3 SPP1000 2.1 mu_fw Breaks MOD Light Programs

The 2.1 mu_fw shipped with the 2.1 release of test station diags causes /spp/scripts/mod_all_on and /spp/scripts/mod_all_off the function incorrectly. This problem has been fixed and new mod_all_on(off) scripts will be shipped in 2.2 of the diags. Until 2.2 is released, you can use the following scripts to turn on and off the MOD.

mod_all_on

```
#
# turn all MOD lights on
#
mput 0xf0fcf210 32
```


6.4.3 SPP1000 2.1 mu_fw Breaks MOD Light Programs (continued)

```
mput 0xf0fcf214 0xffffffff
mput 0xf0fcf218 0xffffffff
mput 0xf0fcf21c 0xffffffff
mput 0xf0fcf220 0xffffffff
mput 0xf0fcf224 0xffffffff
mput 0xf0fcf228 0xffffffff
mput 0xf0fcf22c 0xffffffff
mput 0xf0fcf230 0xffffffff

mput 0xf0c0f014 0xf0fcf210
```

mod_all_off

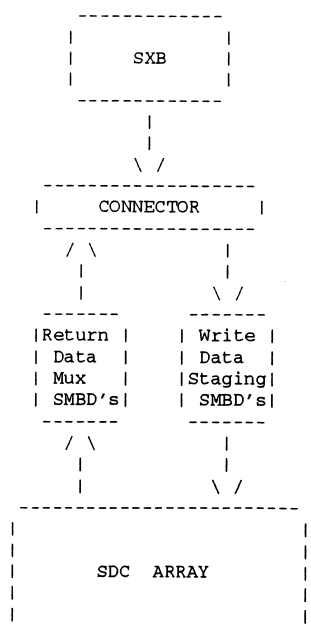
```
#
# turn all MOD lights off
#
mput 0xf0fcf210 32

mput 0xf0fcf214 0x00000000
mput 0xf0fcf218 0x00000000
mput 0xf0fcf21c 0x00000000
mput 0xf0fcf220 0x00000000
mput 0xf0fcf224 0x00000000
mput 0xf0fcf228 0x00000000
mput 0xf0fcf22c 0x00000000
mput 0xf0fcf230 0x00000000

mput 0xf0c0f014 0xf0fcf210
```

6.4.4 C4600 Memory Failure Analysis

Most memory related failures look alike and will generally indicate SDC involvement. But this does not necessarily mean that the SDC is actually at fault. As with all C-Series systems, it is necessary to understand the system architecture, to properly evaluate a given failure. This is because the failures are not necessarily reported in the order of the data flow.

To understand data flow, on the SMB, a block diagram is included bleow:

6.4.4 C4600 Memory Failure Analysis (continued)



Below is an example of a harderror, reported by the SMB:

```
 Hard error Summary

 ------------------------------------------------------------------------
 EVENT #      BOARD     ERROR #     EXTRACTOR
 -------      -----     -------     ---------
    1         MB0       0116108     sdcc.hard_error
 ========================================================================
 mbs0:bank8.sdcc_0_hard_error = 1      mbs0:bank8.sdcc_1_hard_error = 1
 mbs0:bank8.sdcc_0_ext_hard_err = 1    mbs0:bank8.sdcc_1_ext_hard_err = 1
 mbs0:bank8.sdcc_0_soft_is_hard = 0    mbs0:bank8.sdcc_1_soft_is_hard = 0

 An SDCC on mbs0 bank8 detected a HARD ERROR

 ------------------------------------------------------------------------
 EVENT #      BOARD     ERROR #     EXTRACTOR
 -------      -----     -------     ---------
    2         MB0       0116308     sdcc.parity_error
 ========================================================================
 mbs0:bank8.sdcc_0_hard_error = 1      mbs0:bank8.sdcc_1_hard_error = 1
 mbs0:bank8.sdcc_0_par_hard_err = 1    mbs0:bank8.sdcc_1_par_hard_err = 1
 mbs0:bank8.sdcc_0_lock_err_log = 1    mbs0:bank8.sdcc_1_lock_err_log = 1
```


Parity error information logged by the bank8 SDCC gate arrays:

Register name	Ring value				Description
sdcc_1_el_bus_data<31:0>	45	83	2a	b8	BANK8_SMBD.DATA<63..32>
sdcc_1_el_bus_par<0:3>	0	0	0	0*	BANK8_SMBD.DATA<64..67>
sdcc_1_el_row_addr<11:0>			977		BANK8.ADDR<11..0>
sdcc_1_el_row_addr_par			1		BANK8.ADDR_PAR
sdcc_1_el_col_addr<11:0>			022		BANK8.ADDR<11..0>
sdcc_1_el_col_addr_par			1		BANK8.ADDR_PAR
sdcc_1_el_req_type<1:0>			2		BANK8.TYPE<1..0>
sdcc_1_el_zone_hi<3:0>			0		BANK8.ZONE<7..4>
sdcc_1_el_zone<3:0>			f		BANK8.ZONE<3..0>
sdcc_1_el_zone_par			0		BANK8.ZONE_PAR
sdcc_0_el_bus_data<31:0>	c1	1b	09	08	BANK8_SMBD.DATA<31..0>
sdcc_0_el_bus_par<0:3>	1*	1	1	0	BANK8_SMBD.DATA<68..71>
* indicates a parity error					
smbd_write_checksum_msw	8c		68	d6	b2 MB0 wd_xor<63..32>
smbd_write_checksum_par	0		0	0	0 MB0 wd_xor<64..67>

parity type	ODD	ODD	ODD	EVEN	type for each byte
smbd_write_checksum_lsw	ea	17	f9	79	MB0 wd_xor<31..0>
smbd_write_checksum_par	1	1	1	0	MB0 wd_xor<68..71>
parity type	EVEN	ODD	ODD	ODD	type for each byte

The SMBD write data xor checksum parity types are MIXED.
The SMBD xor checksum DOES indicate a write data error on MB0.

Each SDC has two sdcc, which are used to detect and correct single bit and multibit data errors. These sdcc's are deployed in a manner that allows detection on both halves of the SDC. This has the additional benefit of determining if the fault may have occurred prior to, or on the SDC, itself.

The following external error report exists to try and determine the side in error:

```
  mbs0:bank8.sdcc_0_ext_hard_err = 1   mbs0:bank8.sdcc_1_ext_hard_err = 1
```

If the ext_hard_err exists on one side, it is strong evidence that the failure involves the other side, of the SDC. In other words the fault is most likely to reside with the SDC, itself.

When both sdcc's detect the error, then this is a strong indicator that the error exists prior to the SDC. This means that the failure can be anything from a CPU, to SXB, or SMB, itself.

Further evidence of a failure, off the board, or the SMB itself, is the smbd_write_checksum. In this case, all SMBD's should have the same type parity, probably all EVEN. In the case above, this parity is not identical, indicating that the failure rests either external to the SMB, or with the SMBD's, or connector. In this situation, moving the SMB to another location would be a logical step in fault isolation.

If the failure follows the SMB, then the problem is obviously with the board. Otherwise, more analysis will be necessary, with a defective sxbd being a likely target.

FIELD SUPPORT TECHNICAL BULLETIN

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Contents of this issue:

1. Release of FMI-108-A for SP1000/CD's

6.5.1 Release of FMI-108-A for SP1000/CD's

The following was added to the effectivity list.

Possibly all SPP1000/CD systems in the Field shipped during the late Summer or early Fall of 1994. If you suspect you have one from that time period you need to visually inspect the filter cover to see if it is the one in question. The suspect filter cover is P/N 325-000050-500 and has a small step at the power supply end of the cover. Some CD's, shipped during this period and into the Fall, were shipped with a cover that did not have a step, P/N 325-000050-500 Rev A, they are not to be changed. The replacement cover is P/N 325-000050-501.

To visually inspect the cover you can either remove one of the cable plates on the back of CD and with a flashlight, look down into CD to check or you can remove the system cover and then inspect it. Once you have identified that you have the suspect filter cover, you need to contact Convex Logistics FMI Coordinator for the replacement.

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Contents of this issue:

1. Metrum RSP-2150 PM Schedule
2. DLT Service Information
3. C4600 Soft Error Handling
4. Runaway errintd process, with C4600's
5. Metrum RSP-2150 Firmware Requirement

6.6.1 Metrum RSP-2150 PM Schedule

Metrum has revised their Preventive Maintenance Schedules. The following list contains the revised schedule.

Interval	Item	Action	Level
50 Hours Head Time#	Transport Tape Path	Clean	Operator
	External Case	Clean	Operator
1000 Hours Head Time or 20,000 Cartridge load, or 20,000 Wrap Count.	Transport Assy.	Lube	Qualified Tech.
	Head Cleaning Roller	Replace	Qualified Tech.
	Upper Scanner	Clean	Qualified Tech.
	Transport Tape Path	Detailed Cleaning	Depot Svc. Center
3000 Hours Head Time, or 50,000 Cartridge Load, or 50,000 Wrap Count	Upper Scanner##	Replace	Depot Svc. Center
	Capstan Pinch Roller	Replace	Depot SVC. Center
	Loading Belt	Replace	Depot Svc. Center
	Pinch Cam	Replace	Depot Svc. Center
	Takeup/Supply Reels	Replace	Depot Svc. Center
	Main Brakes	Replace	Depot Svc. Center
	Loading Cam Gear###	Replace	Depot Svc. Center
	Tape Path	Alignment	Depot Svc. Center
6000 Hours Head Time, or 100,000 Cartridge Loads.	Lower Scanner	Replace	Depot Svc. Center
	A/C Head	Replace	Depot Svc. Center
	Erase Head	Replace	Depot Svc. Center
	Incline Bases	Replace	Depot Svc. Center
	Mode Switch	Replace	Depot Svc. Center
	Reel Motor Assy.	Replace	Depot Svc. Center

Read 'Drum Mtr Hours' for Head Time
Replacement based on Head Time
Replacement based on Wrap Counts

6.6.2 DLT Service Information

Convex now offers the ATL Products ACL2640 automated tape library. The ACL2640 provides data archival and backup capability using high-performance robotics and up to three DEC DLT2000 cartridge tape drives.

If you require further information about this unit for facilities planing, please order the service plan for this product, document number 0.81-025130-000.

If you are advised that your customer may be receiving only the DEC DLT2000 series drives for use, please direct all questions to our Specials group.

FIELD SUPPORT TECHNICAL BULLETIN

6.6.3 C4600 Soft Error Handling

The C4 introduces two new methods of error handling, to the C series architecture. These are assisted error handling and processor soft error handling. The C-series has previously handled memory and IA related soft errors, but now this is extended to the processor.

The soft errors are those that can be corrected by error correction hardware on an operational system. These errors are logged in the CDB, like the memory, or IA soft errors and can be read with the dump_soft_log utility.

If a soft error is detected by the hardware and error correction hardware is available then the hardware will correct the soft error without interuption. Otherwise, a soft error or an assisted error is detected by errintd. An assisted error will hang the processor.

Assisted errors are errors on the PR boards that cannot be corrected without assistance from the SPU. With these type of failures, errintd scans the PR board for the type of error, corrects it, and then brings the PR back online. If the error is not correctable, it is treated as an APR error if it's enabled, or as a hard error if APR is not enabled. These errors are logged to the file /diag/data/asst_log.

The Assisted errors that can be fixed are data cache assisted error, scalar microcode assisted error, SLIP internal microcode assisted error and vector dispatch assisted error.

Diagnostic release, v1.0.2, enable the soft and assisted errors, for the first time, by entries in the Configuration Data Base, as follow:

```
cu_error_enable =   00000004
ia_error_enable =   00000004
mb_error_enable =   00000004
mb_dc_error_enable =   00000004
pr_error_enable =   00000002
xb_error_enable =   00000002
errintd_option_enable_errors =   00000001
errintd_option_assists_enabled =   00000001
errintd_option_apr_enabled =   00000000
```

The term "soft_is_hard" indicates that soft errors are treated as hard errors and will crash the system. This is the mode that all errors were set to, prior to v1.0.2.

The following extractors, will be treated as assisted errors:

```
sap.MI_dcache_parity_error
sap.uinst_immediate_parity_error
sap.uinst_parity_error
```

slip.uinst_parity_error
svpc.A_cs_parity_error
svpc.B_cs_parity_error
svpc.C_cs_parity_error
svpc.L_cs_parity_error

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6.6.3 C4600 Soft Error Handling (continued)

The following will be handled, as soft errors, when not set to soft is hard:

sap.MI_data_parity_error
sap.MI_dcache_parity_error
sap.MI_isolation_parity_error
sap.X_operand_parity_error
sap.Y_operand_parity_error
sap.Z_operand_parity_error
sap.dispatch_instr_parity_error
sap.uinst_immediate_parity_error
sap.uinst_parity_error
sdiv.X_operand_parity_error
sdiv.Y_operand_parity_error
slip.btab_parity_error
slip.icache_parity_error
slip.uinst_parity_error
slip.valid_parity_error
smd.VXM_address_parity_error
smd.VXM_isolation_parity_error
smd.active_cache_parity_error
smd.inactive_cache_parity_error
smd.mem_address_parity_error
smd.mem_ctl_parity_error
smd.ret_ctl_queue_parity_error
smd.ret_data_queue_parity_error
smd.sap_isolation_parity_error
smd.ssp_isolation_parity_error
smd.xbar_isolation_parity_error
ssp.MI_dcache_parity_error
ssp.MI_isolation_parity_error
ssp.Y_operand_parity_error
ssp.Z_operand_parity_error
ssp.dispatch_instr_parity_error
ssp.uinst_immediate_parity_error
ssp.uinst_parity_error
svrf.A_pipe_parity_error
svrf.B_pipe_parity_error
svrf.C_pipe_parity_error
svrf.MXV_byte_parity_error
svrf.MXV_isolation_parity_error
svrf.VMP_byte_parity_error

The meaning of the CDB entries are as follow:

EN_NONE	0	- soft is hard, hard disabled
EN_SOFT_ONLY	1	- soft logged, hard disabled
EN_SOFT_IS_HARD	2	- soft is hard, hard enabled
EN_HARD_ONLY	3	- soft not logged, hard enabled
EN_ALL	4	- soft logged, hard enabled

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6.6.4 Runaway errintd process, with C4600's

It is possible for the hard_err_mask to get cleared and result in the errintd process rising to 92% of spu, cpu time. This will cause everything, on the spu to run very slowly, as there are no cycles left.

This situation is set up by either a failed attempt at handling an assisted error, or a poorly executed system shutdown.

It is very easy to recover from this, by killing the errintd process and allowing it to restart itself. This will recreate the hard_err_mask and automatically restart errintd. On rare occassions, it is possible that the mask will not be created properly. For this reason the mask should be checked, following this exercise. This can be accomplished as follows:

```
spu> get hard_err_mask
 VALUE: 16#00005392
  |31|30|29|28#27|26|25|24#23|22|21|20#19|18|17|16
  |         Reserved      # APR_ENABLE#HALT |SE|Z1

  |15|14|13|12#11|10|9|8 # 7|6| 5 | 4 # 3 | 2 | 1 | 0
  |Z0|CU|  |IA#X1|X0| |XB#     MB     #      PR
```

Naturally, the mask will vary according to the configuration.

In some instances, it may be necessary to restart the errintd manually and this can be accomplished by: start_errintd -e.

This problem will be corrected in diagnostic release v1.0.3.

6.6.5 Metrum RSP-2150 Firmware Requirement

A recent release of Unitree s/w, version 2.0, has made it a prerequisite that the RSP-2150 drive firmware be at the following level.

```
          Buffer Manager Firmware: V05.17
        Drive Controller Firmware: V05.05
    Mechanism Controller Firmware: V02.14
        Servo Controller Firmware: V01.12
```

This new release of s/w is currently only being shipped as a BETA release to selected sites, and these sites should receive advance warning of the need for this new microcode.

Drives received from Metrum over the past few months have shipped with this level of firmware, so you should check you drives prior to requesting the new firmware.

The one problem at the present is that this new release of firmware is not readily available. Discussions with Metrum are in progress as to how to

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Contents of this issue:

1. SPP1000 mu_config "scrub" Bit Should be On

6.7.1 SPP1000 mu_config "scrub" Bit Should be On

The "scrub" bit in mu_config enables MU scrubbing of memory single bit ecc errors. When running SPP-UX, this bit should be set in all nodes running mu_fw 1.3 or higher. This bit should be turned off when running sppring.

To set the bit:

```
ccmu
ccmu> up
ccmu> put mu_config 0x1
ccmu> down
ccmu> push                #save in NVRAM
ccmu> quit
do_reset 3
```

To clear the bit (for diags):

```
ccmu
ccmu> up
ccmu> put mu_config 0x0
ccmu> down
ccmu> quit
do_reset 3
```

After running diags restore mu_config:

```
ccmu pull <cr>
do_reset 3
```

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Contents of this issue:

1. Release of FMI0107-A for 2-4 node SPP1000/XA's
2. Solution for SPP software upgrades, with no net
3. C3800 SP Softerrors
4. IDC Informational Message

6.8.1 Release of FMI0107-A for 2-4 node SPP1000/XA's

FMI0107-A has been released.

Changes from FMI0107:

Pre-Requisites changed from NONE to Test Station Diags 2.2 or higher.

The Test Station Diag patch tape has been removed from the Required Parts List.

Minor drawing corrections.

6.8.2 Solution for SPP software upgrades, with no net

During any SPP OS installation, problems may arise if there is no active FDDI network, on the system complex. Early on in the install process, it will be necessary to start the swagentd. This will be executed as follows:

```
# /usr/sbin/swagentd
```

If no network exists, this command will be followed, immediately, by the following:

```
ERROR:   swagentd exiting due to initialization error in background
         process.  Check the logfile "/var/adm/sw/swagentd.log" for
         more information.
```

If an active network is available, it will be necessary to install it, before proceeding. If one is not available, it is possible to resolve this issue, with a FDDI loopback connector. Such a loopback connector exists, with the C-Series FDDI controller. If there are no local C-Series systems, with FDDI installed, it is possible to obtain this connector by part number 312-000500-001.

This MIC connector can then be inserted on the FDDI connector, on node 0, located at the very top of the backplane. Upon insertion of the loopback connector, the RINGOP LED should illuminate.

After installation of this loopback, it will be necessary to reboot, to enable the network and proceed with the installation.

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6.8.3 C3800 SP Softerrors

It is possible to encounter SP soft errors, on a C3800. These errors are displayed on the console and saved in the soft_log, on the SPU, if the 8247 NSP and 3240 XCL are in the system configuration.

The other NSP's will handle the soft errors, but they will not be reported and logged. With the above components installed logging will take place.

The SP soft errors are reported in the event of a purge ram parity error. They should be ignored, unless the number logged is excessive. This will normally be the case if the customer complains of these messages scrolling on the Console screen. These errors will not indicate a NSP, but this can be determined from the soft_log.

This is not meant to suggest that there is any specific advantage, to logging, It is only intended to explain the SP soft errors.

6.8.4 IDC Informational Message

The following messages indicate that a disk drive has issued an interrupt, to the IDC, that was not caught. In other words, before the IDC could handle the interrupt another interrupt has received from another drive. Thus making it impossible to identify the drive that issued the first interrupt.

```
[CCU34@18:17:20] ERROR: Request interrupts failed on channel 0. Drive
 failing?
[CCU34@18:24:13] ERROR: Request interrupts failed on channel 1.  Drive
 failing?
```

At this point, the IDC begins to poll the drives in order to match the interrupts with their owner. THis is of very little consequence, except that the IDC continues in polling mode, until the system is rebooted. This can have an impact on performance.

These messages, when seen, will generally appear at boot, but can be experienced, at any time.

It should be understood that this is normally a very intermittent problem and should cause no major problem, for the customer. A bug has been created, for this problem and should be resolved.

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Contents of this issue:

1. PETS Released for C4600

6.9.1 PETS Released for C4600

The first release of C4600 PETS is finally available. The released version is v1.9 and will work on C4's only. This release is not intended for any other C-Series Product. The part number is: 760-002715-007.

This release will be, automatically, distributed to FE's with, current, C4 responsibilities.

The primary difference between this release and previous PETS releases, is that parts 3 and 4 have been added to test the additional vector functionality, 16 VR's.

In addition part 4 will require 1.3 GB of virtual memory, per head. This should not present a problem for standard configurations, which have a 1GB MB, for each processor. For systems with 512MB memories, or more processors than MB's, this may require allocating additional swap space, to run the tests.

If no additional swap space can be found, then it will be necessary to run the fast, or fast.marg scripts, rather than the standard runxx, or systems scripts.

FIELD SUPPORT TECHNICAL BULLETIN

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Contents of this issue:

1. METRUM RSP-2150 Drive PM
2. SPP H/W Class Notes
3. SPP1000 "sppring" Failures

6.10.1 METRUM RSP-2150 Drive PM

Technical Bulletin 6.6.1 has been revised, but not reissued.

The original release of this bulletin contained no notation of any replacement actions for the 2,000 head hour pm, after it's time value was increased to 3,000 head hours. This has been corrected.

To obtain your revised copy, please reprint Technical Bulletin 6.6.

6.10.2 SPP H/W Class Notes

Version 7.5 of the SPP Hardware Maintenance class notes has been placed in:

"/common/tachwbul/spphwman"

All of the files are in Postscript format and are broken out into chapters. Following is a list of the files:

```
Spp.Cover.ps ------------ Cover page
Spp.ClassTOC.ps --------- Table Of Contents
Spp.ClassLOF.ps --------- List Of Figures
Spp.Chap1.ps ------------ Chapter 1
Spp.Chap2.ps ------------ Chapter 2
Spp.Chap3.ps ------------ Chapter 3
Spp.Chap4.ps ------------ Chapter 4
Spp.Chap5.ps ------------ Chapter 5
Spp.Chap6.ps ------------ Chapter 6
Spp.Chap7.ps ------------ Chapter 7
Spp.Chap8.ps ------------ Chapter 8
Spp.Chap9.ps ------------ Chapter 9
Spp.Chap10.ps ----------- Chapter 10
Spp.Chap11.ps ----------- Chapter 11
Spp.Chap12.ps ----------- Chapter 12
Spp.Chap13.ps ----------- Chapter 13
Spp.Chap14.ps ----------- Chapter 14
Spp.Chap15.ps ----------- Chapter 15
Spp.Chap16.ps ----------- Chapter 16
Spp.Chap17.ps ----------- Chapter 17
Spp.appendices.ps ------------ Appendices

Spp.Class.ps ------------ The book as one file
```

6.10.3 SPP1000 sppring Class 9 and 10 Failures with 1 Landmark

If you are running sppring version 2.1.2 and you have 2 nodes connected together and only one of the nodes has a landmarc, sppring will fail class 9 or 10 if the landmarc is in node 0. If the landmarc is in node 1 the tests will run fine. If the landmarc, in node 0, is deconfigured the test runs fine also.

Here is the failure that you get if only node 0 has a landmarc.

```
  > NODE 1 MAUI detected a MURI read parity error
  >
  >       err_glob.error_sticky_csr[12] = 1
```

We do not know if this failure occurs in earlier versions of sppring.

Thanks to the folks in manufacturing for this info.

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Contents of this issue:

1. SPP1200/XA Site Prep. Info.

6.11.1 SPP1200/XA Site Prep. Info.

The SPP1200/XA uses a single phase, 208 VAC, 30 amp circuit.
The power cord and connector are rated at 30 amps.

For domestic systems, the plug is a L6-30P. The recepticle would be a L6-30R(wall mount) or L6-30C(connector for the end of a cord).

International systems will be shipped without a plug.

All other Site Prep. info can be found in the "Exemplar Site Prep. Guide" First Edition. Convex order number DHW-500.

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Contents of this issue:

1. Metrum RSP-2150 Drives
2. Elite III (DKD-505) Configuration
3. Metrum RSP-2150 Microcode Upgrade
4. ER-90 Head Changing Check List
5. Metrum RSS-600 Robot Manual
6. C-Series FDDI OS Incompatibility
7. C4600 SDC Isolation Problem
8. C4600 Memory Extractor Explanation

6.12.1 METRUM RSP-2150 Drives

Metrum has released some information concerning a test that is designed to test the operation of the P5 arm, located inside an RSP-2150 drives transport mechanism, after their analyses of damage done to some customer tapes.

Quote:-

The P5 arm that is shown on the next page, (unable to reproduce this in a text form so a reference source will be supplied), sometimes fails to return completely to it's stop post.

To test the P5 arm, the top cover of the RSP2150 must be removed.

Before inserting a tape, inspect the P5 arm to see if it is touching the stop post. If the P5 arm is not touching the stop post, the RSP2150 should be returned for repair.

To test the P5 arm with a cartridge the RSP2150 must be put into primitive mode. This can be done by putting switch 1 on the Drive Controller to position 6 on, & the rest off, with the RSP2150 off & then turned on.

Insert the cartridge & then eject the cartridge, by rotating switch 2 on TTP circuit card (the TTP is on the right side of the tape transport) to E & back to 0. Do this several times & if the P5 arm ever fails to return to the stop post, the unit should be repaired.

To take the RSP2150 out of primitive mode put switch 1 position 6 back to off & position 1 back to on position, on the Drive Controller. Also make sure the switch 1 on the TTP is back to 0. Then cycle power on the RSP2150.

End Quote.

If you attended any of the Metrum training classes that have been conducted over the years, you will be able to locate a diagram of the P5 post's position in the "Introduction" section of the "METRUM RSP-2150 Operation and Maintenance" manual. This manual has no part number.

If you are unable to locate this diagram, please contact "tachwsup" and one will be faxed to you.

FIELD SUPPORT TECHNICAL BULLETIN

6.12.2 Elite III (DKD-505) Configuration

The I/O board jumper block pin assignment table in the Convex Elite 3 Disk Drive Service Guide, First Edition, incorrectly shows jumper settings for the W3 and W4 blocks.

While you should never have to change these jumpers on a drive received from Dallas, the Service Guide should be corrected.

Following are the revised Table 5 listings for the jumpers in question:-

Block	Jumper	Pins	Description	Default configuration
W3	W3-1	1&3	Microcode configuration bit 2	Not Installed
W3	W3-2	2&4	Microcode configuration bit 3	Not Installed
W4	W4-1	1&3	Microcode configuration bit 0	Installed
W4	W4-2	2&4	Microcode configuration bit 1	Not Installed

Please correct your manuals to reflect these changes.

6.12.3 Metrum RSP-2150 Microcode Upgrade

A new release of microcode is available for the Metrum RSP-2150 drive.

This release, version 5.2, is a co-requisite for sites upgrading to Unitree software version 2.0.

This firmware release incorporates several bug fixes, including corrections to several miscellaneous positioning commands, modification to mode select data, and a change to the ECC rewrite threshold.

The upgrade kits can be ordered through you local logistics office.

The part number for the new microcode release is:- 207-000023-008.

YOU MUST send the serial numbers of any drives that will be upgraded to Paul Marshal(pmarshal), so that Metrum can be advised and track units, and YOU MUST return the old firmware proms to Dallas.

FIELD SUPPORT TECHNICAL BULLETIN

6.12.4 ER-90 Head Changing Check List

The following chart is provide to assist with the steps needed to correctly replace and adjust a read, or write head in an ER-90 drive unit.

Head to Replace		
Install both heads	X	
Install AST head only		X
Install Wrt head only	X	

Steps to Replace Head	AST	Data Pattern	Tracking	Record Optimize	Equalizer
Remove & Replace AST head Vol 1 Sec 13-8, p13-7	1	1			
Remove & Replace Wrt head Vol 1 Sec 13-7, p13-6	2	1			
Set Record Drive to Midrange (170) Vol 2 Sec 8-11, p8-6	3	2 off	pseudo 1	auto manual	n/a
Adjust Ramp & Offset Vol 1 Sec 14-23, p14-35	4	2 3 off (offset) field (ramp)	pseudo 1	auto n/a	n/a
Record Optimize Vol 2 Sec 8-11, p8-6	5	3 4 field	pseudo 1	auto auto	n/a
Verify Coplanarity Vol 1 Sec 14-27, p14-43	6	5 off	pseudo 1	manual n/a	n/a
Adjust Ramp & Offset Vol 1 Sec 14-23, p14-35	7	6 off (offset) field (amp)	pseudo 1	auto n/a	n/a
Center equalization Vol 2 Sec 8-12, p8-6	8	4 7 field	pseudo 1	auto n/a	manual
Set levels, Equalizer Vol 2 Sec 8-15, p8-7	9	5 8 field (DPG all 1's)	Nyquist	auto n/a	manual
Adjust Equalization Vol 2 Sec 8-16, p8-7	10	6 9 field	pseudo 1	auto n/a	auto/manual
Optimize SER Vol 2 Sec 8-17, p8-9	11	7 10 field	pseudo 1	auto n/a	auto

EMASS Tech. Bulletins # 028, and 029 should be used for some of the adjustments.

6.12.5 Metrum RSS-600 Robot Manual

An error has been reported in the Metrum Technical Manual for the RSS-600b Automated Tape Library.

The following change should be made to item 7 of the 5.7.1 PULSE MOTOR description, on page 5-59.

Change the two line to read:-

* Drum pulse - Pulse Motor Controller CCA #1 for a minimum cycle width of 40usec. *****

* Handler pluse _ Pulse Motor Controller CCA #3 for a minimum cycle width of 2.1 msec. *****

Text underlined with "*******" are the required changes.

6.12.6 C-Series FDDI OS Incompatibility

The C-Series FDDI Vendor has upgraded the firmware on all FDDI controllers, that are being shipped to CONVEX. It has been changed from vA-19, from A-11.

This creates an incompatibility with the existing firmware files, in all C-Series OS releases.

For this reason, a new firmware download file has been placed in /common/tachwsup/fddi.x00. This file should then be placed in the /mnt/os directory, on the SPU. This file is backward compatible with all previous hardware.

It is recommend that this be accomplished immediately, for all systems with FDDI currently installed, immediately. It should be understood that files are only available in /common for a limited time and this will disappear on 03/31.

If this is not accomplished, then any system requiring a replacement FDDI controller will fail, in the following manner:

```
[CCU03@09:53:51] LAN-208 VMEbus 0 controller is not present at CSR 0x6000
[CPU01@09:53:51] Device "LAN-208" (3/0/0x6000 int 7) FAILED (error -1)
[CPU01@09:53:51] Unit   "fd" unit number 0
[CPU01@09:53:51] fdattach: controller configure failed, attach aborted
[CPU01@09:53:51] Unit   configure error -1
[CPU01@09:53:57] Device "LAN-208" (3/1/0x6000 int 7) Slot=3
drvfsd: downloading "fddi.x00" to CCU 3
[CPU01@09:53:58] Unit   "fd" unit number 0
drvfsd: start>**************************************************<end
[CCU03@09:54:16] fd0:fd_exec_fw: failed
[CCU03@09:54:16] fd0: ** WARNING ** using ROM resident firmware
[CCU03@09:54:16] fd0: Firmware version V4211/2211 A17 .
[CPU01@09:54:16] Firmware Version V4211/2211 A17 .
[CPU01@09:54:16] fd0: address = 00:00:77:84:9b:39
[CPU01@09:54:17] fd0: hardware network address = 00:00:ee:21:d9:9c
```

For upgrades and new systems, this will be handled by way of tacpatch

2.0.129.

6.12.7 C4600 SDC Isolation Problems

It has been determined that, in many cases, the error extractor, sxbc.mem_data_parity_error, does not provide enough information. Specifically, it is not possible to determine which SDC the data was returned from, as in some cases the failure will be a defective SDC.

To locate the source SDC, we need to re-enable the SMB and execute rcque directly after the failure. The procedure would be as follows:

```
  1) spu> ddb
     [DDB]-> $dcpu x   <where x is equal to cpu>
     [DDB]-> $rcque
```

This would have to be done for each processor installed.

NOTE If no parity error exists, for any processor, it indicates that the data was destined for the SIA. In this case, no action can be taken until the next event.

The return will be as follows:

```
                         MI_RET_Q Dumper V0.1
                CPU0 Dump of the Mem Interface Return Queue
SMC  +- AddrQ + +------- CntlQ -------+ SMD +--- DataQ -----+ +---- CntlQ ----+
                           R
                         T e L
                         h u a                                Logical
Queue Logical    St      r s s Dest Req    Req     Data     Data       Addr  Req  Req
Addr Addr<31:0> Cnt      d e t Reg  Type   Size   <63:32>  <31:00>    <14:0> Type Size
=================================================================================
  00  00000000  000 0 0 1 T16  VP     WD     00000000 00000001     3008  SP    LW
  01  00000000  000 0 0 1 T17  VP     WD     00000000 00000000     0008  SP    LW
  02  00000000  000 0 0 1 T18  VP     WD     00000000 00000000     0008  SP    LW
  03  00000000  000 0 0 1 T19  VP     WD  rw>01ffc810 00000000     0008  SP    LW
  04  01ffc810  000 0 0 1 T20  VP     WD     00000000 00000000     0008  SP    LW
  05  00000000  000 0 0 1 T21  VP     WD     00000000 00000000     1000  IP    LW
  06  00000000  000 0 0 1 T22  VP     WD     00000000 00000000  rw>1008  IP    LW
  07  00000000  000 0 0 1 T23  VP     WD     00000000 00000000     1010  IP    LW
  08  00003008  000 0 0 1 S31  SP     LW     7f144080 8abcd000     1018  IP    LW
  09  0000000c  000 0 0 1 S31  SP     LW     7f144100 8abca000*    1020  IP    LW
  0a  0000000c  000 0 0 1 S30  SP     LW     7f183804 00000000     1028  IP    LW
  0b  0000000c  000 0 0 1 S29  SP     LW     7f7850c0 00000020     1030  IP    LW
  0c  0000000c  000 0 0 1 S28  SP     LW     7f80b0c6 10000000     1038  IP    LW
  0d  8abc9000  000 0 0 1 T31  IP     LW     7f82b006 00000000     1040  IP    LW
  0e  8abc9008  000 0 0 1 T31  IP     LW     7f02fffe 00000000     1048  IP    LW
  0f  8abc9010  000 0 0 1 T31  IP     LW     7f185904 fffffff8     1050  IP    LW
```

As can be seen, the parity error is designated by the *. As the bad data is located 6 que locations below the rw pointer, it's necessary to move the same number of locations below the pointer, for the logical address. This is logical address 1038.

The logical address displayed is bits 0-15 of the address. The bank can be located in bits 3 through 7. This means that the bank in error is bank 7.

This dump is being added to this extractor, as of the next diagnostic release, v1.0.3.

6.12.8 New C4600 Memory Extractor Explanation

As previously described, the extractor sxbc.mem_data_parity_error is somewhat flawed, as it does not report the bank involved in this type of memory error, reported by the crossbar.

In an attempt to improve the extractor and collect additional information, this extractor will be enhanced in the v1.0.3 Diag release. Because of the necessary changes, an explanation is necessary.

Below are the changes:

* uses the "cpu_os_req_<0:3>" and "cpu_avail_<0:3>" cdb keys to determine which processors are available and enabled. (Both bits must be set for a given processor in order for this script to "see" it.)

* dumps the mi_ret_q of each processor to a separate file. Each filename has the processor # and date/time information to make it unique. This will prevent it from being overwritten by later failures.

* greps each file for errors. If no error is found the file is removed.

* prints a message about each processor as part of the extractor output. For each processor it will either say that no error was found or it will say that an error was found and give the filename where the contents of the queue have been saved. This will aid in matching a failure in the error log with the corresponding dump file.

Below are the cautions that should be understood, with this extractor:

* running this extractor manually on a machine which has not been fully initialized will cause a coredump. This is because the mi_ret_q dumper coredumps when run on an un-initialized machine with random data in the SMC/SMDs.

* If the read data that causes the parity error goes to the I/O system (SIA) this function will not find the bad data. It will only find it if the data was destined for a processor.

* The bank # is not obvious from glancing at the mi_ret_q output. Some expertise is required in order to obtain the correct bank #. This is explained in the previous tech bulletin.

Below are some sample outputs from this extractor.

1) example of a parity error in a system with 2 processors where one
   of the mi_ret_q dumps contains bad parity:

EVENT #	BOARD	ERROR #	EXTRACTOR
1	XB	0201010	sxbc.mem_data_parity_error

6.12.8 New C4600 Memory Extractor Explanation(continued)

Parity error detected on data from SMB/SCU to SXB.
(mem_hard_error_s)

	Byte								
Field	0	1	2	3	4	5	6	7	Board Signal
m0_rdata_hold<63:0>	44	79	89	97	c6	d6	91	d2	M0_XB.DATA<63:0>
m0_rdata_par_hold<0:7>	1	0	1*	1*	0*	0	0	1	M0_XB.PAR<0:7>
smbd_read_checksum_msw	ff		d3		46		64		MB0 rd_xor<63..32>
smbd_read_checksum_par	1		0		1		1		MB0 rd_xor<64..67>
parity type	ODD		ODD		EVEN		EVEN		type for each byte
smbd_read_checksum_lsw	82		d7		7d		84		MB0 rd_xor<31..0>
smbd_read_checksum_par	0		1		1		1		MB0 rd_xor<68..71>
parity type	EVEN		ODD		ODD		ODD		type for each byte

The SMBD read data xor checksum parity types are MIXED.
The SMBD xor checksum DOES indicate a read data error on MB0.

* indicates parity error

PR0 mi_ret_q DOES NOT contain a parity error.
PR2 mi_ret_q DOES contain a parity error.
contents of queue saved in file /sst/pr2.mi_ret_q.out.032095184937

NOTE
In this case the SMBD checksum indicates that there was bad
parity on data going through the SMBDs. This tends to point
in the direction of a bad SDC. But it's possible for multiple
bit parity errors to get past the checksum without being
detected. In this case a SDC eliminated simply because the checksum
is good.

2) example of a parity error in a system with 2 processors where neither
   of the mi_ret_q dumps contains bad parity:

EVENT #	BOARD	ERROR #	EXTRACTOR
1	XB	0201010	sxbc.mem_data_parity_error

Parity error detected on data from SMB/SCU to SXB.
(mem_hard_error_s)

6.12.8 New C4600 Memory Extractor Explanation(continued)

	Byte								
Field	0	1	2	3	4	5	6	7	Board Signal
m0_rdata_hold<63:0>	44	79	89	97	c6	d6	91	d2	M0_XB.DATA<63:0>
m0_rdata_par_hold<0:7>	1	0	1*	1*	0*	0	0	1	M0_XB.PAR<0:7>
smbd_read_checksum_msw	ff		d3		46		64		MB0 rd_xor<63..32>
smbd_read_checksum_par	1		0		1		1		MB0 rd_xor<64..67>
parity type	ODD		ODD		EVEN		EVEN		type for each byte
smbd_read_checksum_lsw	82		d7		7d		84		MB0 rd_xor<31..0>
smbd_read_checksum_par	0		1		1		1		MB0 rd_xor<68..71>
parity type	EVEN		ODD		ODD		ODD		type for each byte

The SMBD read data xor checksum parity types are MIXED.
The SMBD xor checksum DOES indicate a read data error on MB0.

* indicates parity error

PR0 mi_ret_q DOES NOT contain a parity error.
PR2 mi_ret_q DOES NOT contain a parity error.

In this case the data must have gone to the I/O system. There was no
meaningful information in either of the mi_ret_q dumps.]

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Contents of this issue:

1. SPP Gate Array Torque Check
2. V1.0.3 Diagnostic Release for C4600
3. New SCSI Differential Disk
4. New I/O Diagnostics Released for C-Series
5. QSC Information

6.13.1 SPP Gate Array Torque Check

It is recommended to verify the SPP gate arrays are torqued to 5 in/lbs during system installation. This should be re-checked, during PM, at 90 day intervals.

6.13.2 V1.0.3 Diagnostic Release for C4600

In addition to QSC support, the v1.0.3 diagnostics introduces several enhancements and bug fixes, as follow:

Enhancements:

1) New sxbc.mem_par_err extractor, to isolate memory bank source of data in error.

2) Added several CDB keys, for support of the fault cop, which reports cache slipped locations.

3) Upgraded QPC firmware, to v1.2

4) Upgrade systme ucode to add the fill instruction, add a performance enhancement and change to guassian functions.

5) Hard_logger CXTS flags added, to count number of extractor failures.

Fixes:

1) Fixed the dcache display for the SMC3 and SMD3 gate arrays.

2) resolve intermittent problems seen with downloading ucode, for multiple processors.

3) Fixed errintd to prevent hangs while handling assisted errors.

4) Fixed errintd to enable logging, for all soft errors.

5) Fixed sysreset to clear soft_is_hard SPR fields, if the SMD contains bad locations.

6) BPC firmware is upgraded to 3.21, to fix false fan errors reported by the I/O bay.

6.13.3 New SCSI Differential Disk

The elite9 disk drive is now available, to be used with the new QSC, for C-Series systems, only. This drive is not intended for use with the VME SCSI controller.

The part number, for a formatted drive, without chassis, is 550-002290-297.

The product order number, in the pricebook, is a DKD-506, but the ioconfig entry is DKD-402.

All part number, for this drive, are as follow:

ASSEMBLY	PART NUMBER
ELITE 9 FORMATTED (Disk only No chassis)	550-002290-297
POWER SUPPLY	200-001046-200
FRONT PANEL CONTROL BOARD	411-001460-200
FAN ASSEMBLY	500-000544-200
AIR FILTER	312-000555-001
INTERNAL DATA CABLE	601-680000-200
DC CABLE HARNESS	603-070010-200
AC CABLE HARNESS	603-030042-200
DRIVE TO OPERATOR PANEL	601-240001-200
GROUND STRAP	603-010029-200
SCSI CABLE 1.5'	604-680002-200
SCSI CABLE 10'	604-680002-201

The Elite9 drive is 10.8 GB disk drive, with more than 9GB, after format. It is a 5 1/4" drive, with 27 data heads and 14 platters. The average seek time is 11.5 ms.

The drive is installed in virtually the same chassis, as that used with the DKD-505 drive. The cabinet configuration, will also be the same.

The part number, of the Elite 9 Service Guide, is 081-028130-000 and the the order number is DHW-826.

The max current is 1.1 amps, at 5VDC and 4.8 amps, at 12VDC, for strat. The max operating current is 1.27A 5VDC and 1.94A 12VDC.

The utility scsiutil is the means for format and test of this drive.

6.13.4 New I/O Diagnostics Released for C-Series

New Diagnostics are being released, for the following platforms:

C3200/3400	v2.0 I/O Diags
C3800	v4.2 Diagnostics
C4600	v1.0.3 Diagnostics

The v2.0 release fixes most known I/O diagnostic bugs as well as provide the utilities and support, for QSC. These new utilities include scsiutil an qsc_ldplsi.

The v4.2 release provides only the new QSC support. There are no enhancements, or bug fixes included with this release.

The v1.0.3 release supports QSC, but will add several enhancements and bug fixes. These will be discussed in another tech bulletin.

6.13.5 QSC Information

The QSC (Quad SCSI Channel) has completed the beta phase and will soon be entering production. Because of this, it is necessary to present a brief explanation and discuss the prereq's.

The QSC is a SCSI oriented CCU and complies with SCSI, SCSI-2, F/W and preliminary SCSI-3 specs. It is ultimately intended to support a host of SCSI devices, but will, initially, support only the Elite9, 9GB SCSI disk.

This board is supported on all C-Series systems, with the exception of C1. It is not supported on the SPP series systems.

CAUTION The QSC does not, currently support boot devices. or swap swap devices. Therefore, it cannot be shipped as the only disk subsystem.

Theoretically, the QSC can support up to 15 devices on a single channel, or 60 devices total. This will be limited, at least initially, to 32 total disks, or 8 per port.

The cable and disk configuration will be much the same as the IDC, with some minor exceptions. For instance, the CCU-to-Bulkhead cables will be different from all previous CCU cables. For this reason, the CCU cables will always be replaced, even on the 3800, which may mean a total removal of bay 4, for this installation.

The QSC includes Plsi logic which supports firmware and logic changes on the fly. Thus shortening the upgrade process dramatically. This ucode will be installed, using the ldplsi utility.

The diagnostic support is provided by qsc4000, which in addition to standard logic and onboard tests, includes loopback testing, between the individual ports, for fault isolation.

The drives can be formatted and tested by means of the scsiutil, which is similar to idcfmt. An online man page will be included, with the driver, for this utility.

6.13.5 QSC Information (continued)

The prerequisites are as follows:

1) OS 11.0, or higher
2) Plsi tape
3) QSC driver on a tape
4) C32/3400's
   a) rev 2.0 I/O Diagnostics
   b) PI2 2224 rev G, or 3224 rev E.
5) C3800, v4.2 Diags
6) C4600, v1.0.3 Diags

Part numbers:

QSC board assembly (tested)	550-002447-200
bulkhead to ccu cable	604-680002-200
1ft. 6in. SCSI cable	604-680003-200
10 ft. SCSI cable	604-680003-201
30 ft. SCSI cable	604-680003-202
C2/JAV QSC installation kit	550-001447-211
L-shaped retma rail bracket	320-004608-500
QSC Bulkhead rear emi panel	312-000425-001

Ioconfig entry:

```
  qsc 4
 scsi 0 SCS-021
   unit 0 subunit 0 type DKD-402      sd0
   unit 1 subunit 0 type DKD-402      sd1
 scsi 1 SCS-021
   unit 0 subunit 0 type DKD-402      sd2
   unit 1 subunit 0 type DKD-402      sd3
 scsi 2 SCS-021
   unit 0 subunit 0 type DKD-402      sd4
   unit 1 subunit 0 type DKD-402      sd5
 scsi 3 SCS-021
   unit 0 subunit 0 type DKD-402      sd6
   unit 1 subunit 0 type DKD-402      sd7
```

NOTE Logical assignments are supported, as with the IDC.

Although the device entry is DKD-402, the product is listed as DKD-506.

The max differential cable length is the SCSI limit of 25m, but 30 feet is the longest standard cable.

QSC Service Guide part number 081-026730-00.

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Contents of this issue:

1. SPP Gate Array Torque Check Revised
2. SPP1000/1200 CMC_ERR_EN* Parameter Settings
3. Failures during SPP Power Initialization
4. QSC Diagnostic Failure
5. C4600 Isolation Procedures for Memory Read Errors(continued)
6. SPP1000 4Gb Disk Drive FMI
7. Metrum RSP-2150 P5 Check, Revised

6.14.1 SPP Gate Array Torque Check Revised

It is recommended to verify the SPP gate arrays are torqued to 5 in/lbs during system installation. This should be re-checked, during PM, at 90 day intervals.

Remember to torque the gate arrays in an X pattern.

6.14.2 SPP1000/1200 CMC_ERR_EN* Parameter Settings

The CMC_ERR_EN0 is a mask used to enable CCMC error reporting. If this mask is set incorrectly, some CCMC errors will not be reported when they should. Please verify the CMC_ERR_EN0 parameter is set correctly for each of your SPP systems.

It should be set to:

CSB3	0xfffffff8	244	CMC_ERR_EN0
	0x00000000	245	CMC_ERR_EN1
CSB4 Single-Node (NO SCI)	0xfc7f3fff	244	CMC_ERR_EN0
	0x00000000	245	CMC_ERR_EN1
CSB4 Multi node	0xfd7e3f7f	244	CMC_ERR_EN0
	0x00000000	245	CMC_ERR_EN1
ASB Multi-node (SPP1200)	0xfd7e3f7f	244	CMC_ERR_EN0
	0x40000000	245	CMC_ERR_EN1

You can use ccmu to check and correct the value.

6.14.3 Failures during SPP Power Initialization

It's been discovered that due to procdural changes, with the current teststation software, it is possible to fail, intermittantly, when powering up a node.

The failure will appear as a MU_STATUS_MAUI_TIMEOUT, code 391 and will always contain a MU_INFO value of 0xffeb4xxx, indicating a problem with slice 3.

This failure can be cleared with a do_reset and will not be seen again, until the node is powered down. This will not crash an active node.

This problem is due to the MU timeout value being set too low and will be corrected in the next teststation software release, after v3.0.

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6.14.4 QSC Diagnostic Failure

It is possible to encounter the following qsc4000 diagnostic failure:

```
 Subtest    1     0:02:54   passed  Verify 1032 pLSI programs
 Subtest    2     0:00:58   passed  Verify 2032 pLSI programs
 Subtest 1000     0:00:00           Reset of QSC, EEPROM checksum & versi
 Subtest 1100     0:00:20   passed  Data RAM bit functionality
 Subtest 1110     0:00:00   passed  Data RAM column functionality
 Subtest 1120     0:00:00   passed  Data RAM uniqueness
 Subtest 1130     0:00:00   passed  Data RAM parity
 Subtest 1200     0:00:23   passed  Instruction RAM bit functionality
 Subtest 1210     0:00:00   passed  Instruction RAM column functionality
 Subtest 1220     0:00:01   passed  Instruction RAM uniqueness
 Subtest 1230     0:00:00   passed  Instruction RAM parity
 Subtest 1300     0:00:08   passed  PMAP RAM bit functionality
 Subtest 1310     0:00:00   passed  PMAP RAM column functionality
 Subtest 1320     0:00:00   passed  PMAP RAM uniqueness
 Subtest 1400     0:00:00   passed  PBUS header generation
 Subtest 1410     0:00:00   failed  PBUS access

 *****  Wed Apr  5 12:30:05 1995  *****
 Test:  qsc4000.t  1.12   Class: 1  Subtest: 1410 1.18 Count: 1  Error: 0
 Failed:  PBUS access
      ---------- Trace point: 1410.1 ----------
 Error 0xe: Byte strobe test
 32 bit access. Address 0x00400250 Expected 0x00010203 Actual 0x10000000

 Test 'qsc4000.t' failed
```

6.14.5 C4600 Isolation Procedures for Memory Read Errors

As reported previously, the Crossbar does not indicate the bank source of bad data. This makes it very difficult to determine where a memory failure, as reported by sxbc.memory_par_err, may originate from.

To assist in this, starting with diagnostic v1.0.3, this extractor will save the rcque output, for each head. This extractor makes no attempt at analysis, but leaves that for further analysis.

As the analysis of this information may prove rather complicated, a thorough explantion of this is included below. This, along with previous related tech bulletins should enable the knowledgable individual to, successfully resolve this type of failure.

Below is the return queue information, which will be contained in the /sst/prx.mi_ret_q.out file, created by the new extractor:

6.14.5 C4600 Isolation Procedures for Memory Read Errors(continued)

MI_RET_Q Dumper V0.1
CPU0 Dump of the Mem Interface Return Queue

SMC +- AddrQ +		+------- CntlQ -------+					SMD +--- DataQ -----+		+---- CntlQ ----+	
Queue Addr	Logical Addr<31:0>	St Cnt	Thr	Reu	Las	Dest Reg	Req Type	Req Size	Data <63:32>	Data <31:00>	Logical Addr <14:0>	Req Type	Req Size
00	00000000	000	0	0	1	T16	VP	WD	00000000	00000001	3008	SP	LW
01	00000000	000	0	0	1	T17	VP	WD	00000000	00000000	0008	SP	LW
02	00000000	000	0	0	1	T18	VP	WD	00000000	00000000	0008	SP	LW
03	00000000	000	0	0	1	T19	VP	WD	rw>01ffc810	00000000	0008	SP	LW
04	01ffc810	000	0	0	1	T20	VP	WD	00000000	00000000	0008	SP	LW
05	00000000	000	0	0	1	T21	VP	WD	00000000	00000000	1000	IP	LW
06	00000000	000	0	0	1	T22	VP	WD	00000000	00000000	rw>1008	IP	LW
07	00000000	000	0	0	1	T23	VP	WD	00000000	00000000	1010	IP	LW
08	00003008	000	0	0	1	S31	SP	LW	7f144080	8abcd000	1018	IP	LW
09	0000000c	000	0	0	1	S31	SP	LW	7f144100	8abca000*	1020	IP	LW
0a	0000000c	000	0	0	1	S30	SP	LW	7f183804	00000000	1028	IP	LW
0b	0000000c	000	0	0	1	S29	SP	LW	7f7850c0	00000020	1030	IP	LW
0c	0000000c	000	0	0	1	S28	SP	LW	7f80b0c6	10000000	1038	IP	LW
0d	8abc9000	000	0	0	1	T31	IP	LW	7f82b006	00000000	1040	IP	LW
0e	8abc9008	000	0	0	1	T31	IP	LW	7f02fffe	00000000	1048	IP	LW
0f	8abc9010	000	0	0	1	T31	IP	LW	7f185904	ffffff8	1050	IP	LW

As explained in previous bulletins, the source of the data, in error, can be isolated as follows:

1) The parity error can be located by the asterisk (*) found next to the data.

2) Using this and the "r" pointer located in the same data column, the difference, between the pointer and the parity error should be determined by counting entries, from one to the other. In the example above, the parity error is 6 que entries below the pointer.

3) Using the offset of 6 and moving to the Logical address column, simply count down 6 entries, from the "r" pointer.

NOTE
In the above example, the "r" (read) and "w" (write) pointers are together, forming the rw> pointer. This is not always the case. Insure that the read pointer is always used as the reference.

4) After locating the appropriate entry, 6 down from the read pointer, move "up" to the previous entry, to determine the proper address. This anomaly is due to the way that clocks are stopped, while processing the error.

In other words, the entry 6 down from the pointer is 1038, but the source is actually the 1030 address, found one entry above.

6.14.5 C4600 Isolation Procedures for Memory Read Errors(continued)

5) To determine the source of the data, the following explanation can be used:

The information contained in the Logical Address column, of the Return Que, is bits 0-14 and can decoded from the following chart:

Interleave type	Simm Population	# of SMBs	DRAM row	Board	Bank Select
Mid	Full	1	8	-	7:3
Mid	Full	2	9	5	8:6, 4:3
Mid	Full	4	10	6:5	9:7, 4:3

In the Return Que example above, the address was determined to be 1030. Using this and the chart, it is possible to locate the defective bank and the SMB involved.

Assuming that two memory boards are installed in the system, the SDC can be determined by concatenating bits 8:6 and 4:3. This would be broken down as:

Bit #	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
addr	0	0	1	0	0	0	0	0	0	1	1	0	0	0	0	(0x1030)

Concatenating bits 87643 gives you 00010 which is bank 2.

It should be understood that the SDC (banks) are labeled as decimal. For this reason, values above 9 will have to be converted to decimal, to locate the correct SDC.

6.14.6 SPP1000 4Gb Disk Drive FMI

FMI0109 has been released. This FMI will replace the differential SCSI controllers installed in a SPP node, to allow this node to use the recently released 4Gb disk drives.

The FMI only affects systems that will be installing these new drives that are purchased through Convex.

6.14.7 Metrum RSP-2150 P5 Check, Revised

Technical Bulletin 6.12.1 described a way to check the P5 operation in an RSP-2 Metrum drive. It has been found that this procedure does not work correctly, so a revised procedure follows.

Remove the top cover of the unit in a clean area. Post 5 is the post that wraps the capstan during load, See Ops & Maintenance diagram Transport Top

View.

P5 has a top lip, and it uses stored spring force to return during unloads. Friction can cause this return time to lengthen, which changes a critical clearance for the media over the P3 and Subload posts during unload.

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6.14.7 Metrum RSP-2150 P5 Check, Revised(continued)

P5 has a top lip, and it uses stored spring force to return during unloads. Friction can cause this return time to lengthen, which changes a critical clearance for the media over the P3 and Subload posts during unload.

Using gloves from the PM kit, manually test the return travel of the P5. It should be smooth and an even speed for the full travel. Bad ones will return sharply for most of the travel, but may take a second to complete the last few millimeters. Or may hang briefly along the travel.

Load a scratch tape then use the eject button to unload, or TTP SW2 'E' for unload. Observe the clearance of the media over the P3 post and the Subload post. Repeat the load and unload several times. Tape damage or visible variations in the clearance of the media over the P3 is cause for return to Metrum.

Next check the full path alignment.
Load a tape, then move TTP SW2 from '0' to '7' this will do a full wrap of the capstan, and start foward motion. Check for waves, curling, edge damage especially around P4.
Move TTP SW2 to '6', unwraps, goes into fast foward. Check the media path.
Move TTP SW2 to '1', goes into rewind. Check the media path.
Move TTP SW2 to '0' done.
TTP SW2 is the front rotary switch of the two on the side of the Tape Transport assembly.

Our thanks to Ernie Tibbets for this revised procedure.

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Contents of this issue:

1. New Ethernet SW Warning.
2. C4600 APR Rule.
3. QSC Cabling Considerations.

6.17.1 New Ethernet SW Warning

It should be understood that the driver, for the new Eagle ethernet controller, is included in the 11.1 OS release. This release supports the C4600 architecture. Attempting to install the v1.0 driver, over 11.1, will result in failure.

It will still be necessary to install the diagnostic for this product. A new software kit has been created, for C4 support. The part number is 081-007122-002.

The driver will be required for all 11.0 based systems.

6.17.2 C4600 APR Rules

The cpu_monitor daemon is missing from the production 11.1 OS. For this reason tacpatch 11.0.128.1 exists to load this utility on a C4600. This patch can be found under core utilities and not the OS.

In addition, the cpualloc.test utility is not available on the workstation. For this reason it is not possible for cpu_monitor to initiate sst tests, on a failed head. Because of this it is necessary to set SST_ENABLE = 0, in /etc/cpu_monitor.config file.

The cpu_monitor can then be utilized by placing the following entry at the bottom of the rc.local file:

```
if [ -f /etc/cpu_monitor -a -f /etc/cpu_monitor.config ]; then
     /etc/cpu_monitor &
     echo -n ' cpu_monitor'
fi
```

The final paramter is an entry in the CDB, as follows:

```
errintd_option_apr_enabled =   00000001
```

This should already be set in diagnostic release v1.0.2 and above.

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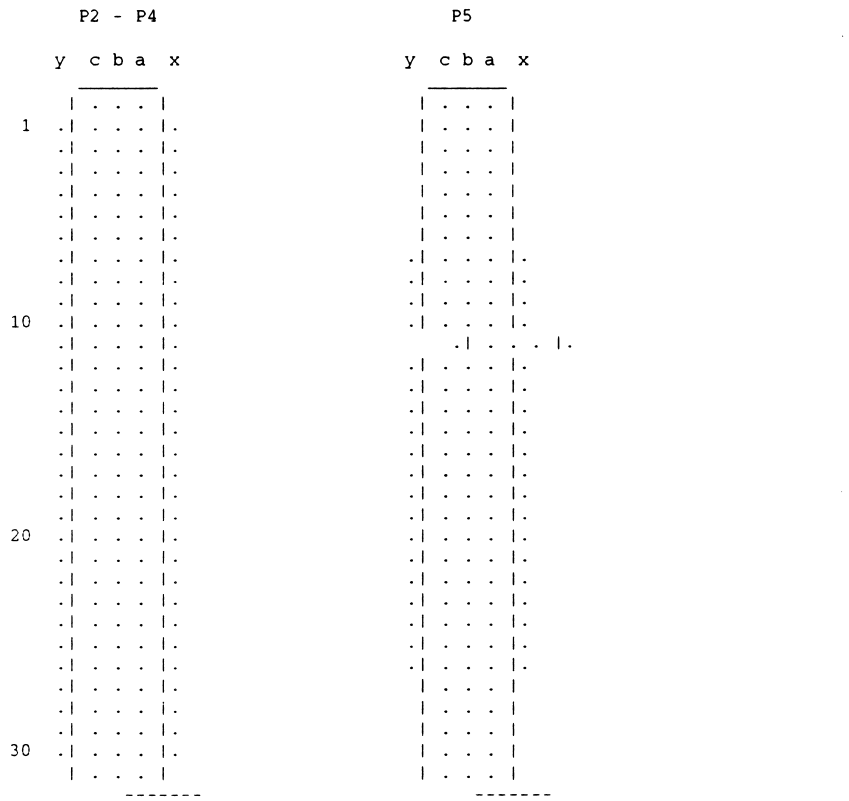
6.17.3 QSC Cabling Considerations

The QSC cables are 32x3 pin connectors, with there being no wires attached to pins on either row 1, or row 32. In nearly all cases, the first row of 3 pins and the last row of 3 pins, are removed, or bent back, in the case of some C2's, for the connectors P2-P4. The connector for P5 is not a problem. For this reason, the correct cable alignment is as seen below:



The top wire should be some shade of violet/red. The bottom wire is brown.

As seen above, there should be no uncovered pins. if the top and bottom row of pins is bent over, then it may be necessary to straighten the pins before installing the cable in P2-P4.

The ground pigtail, attached to the cables, are to be installed over the ground rows, x, or y. The instructions, in the Service Guide call for placing it in row y, left, but it does not matter. If room is available, it can even be installed on row y of an adjacent connector.

Contents of this issue:

1. Testing SPP1000's for PA7100 Problems
2. C3800/QSC and Diag v4.2
3. QSC and the Plsi Explanation
4. C4 Errintd Hang
5. Datatower Diag incompatibility with Screen Enhancer

6.18.1 Testing SPP1000's for PA7100 Problems

These are the instructions for retrieving, installing, testing and reporting the PA7100(tchip) bug test.

All PA7100 CPU modules must tested as soon as possible.

*** Reporting ***

Reporting Data will be compared with all known Complex serial numbers and reminders will be sent to the people that still need to respond.

1) Retrieve the Diagnostics from the designated place. (See Below)
2) Run the Installation portion of these instructions.
3) Email output of diagnostic (/tmp/PAtest/patest.out) to sppchk@convex.com. This info will be parsed and a PR will be created for each failing cpu.
4) Priority you perceive for the Customers Site

*) Email the file patest.out to Dallas to sppchk@convex.com
A filter will parse the information and open a PR in the Viper Database. Be aware that you will receive mail as to the assignment. The Product Code will be PA7100

*** Retrieval ***

Convex Wan

```
ftp lurch
username: ftp
password: your_email_address

cd pub/PAtest
get PAtest.tar.gz
get gunzip.hp
```

Internet

```
ftp convex.convex.com
username: ftp
password: your_email_address
```


6.18.1 Testing SPP1000's for PA7100 Problems (continued)

```
cd tac_patches
get PAtest.tar.gz
get gunzip.hp
```

*** Installation ***

Note: You must be sppuser and it is assumed the files are in /tmp on the teststation.

1. /tmp/gunzip.hp /tmp/PAtest.tar.gz

2. tar xvf /tmp/PAtest.tar

*** Testing ***

1. Shut down SPP-UX.
   sync
   sync
   /etc/reboot

2. If the OBP auto-reboot? flag is true, you will want to set it to false until testing is complete.

3. cd /tmp/PAtest

4. patest <# of cpus in system> | tee -a patest.out
   For a 2 node 16 cpu system the command would be:
   "patest 16 | tee -a patest.out"

HPMC FAILURES

If the diagnostic detects a HPMC(High Priority Machine Check), on a cpu, you will need to disable the failing cpu and run the test again. You will need to continue to disable cpus, that get HPMCs, until the test will pass without a HPMC being detected. See fail.examples for an example of a HPMC failure.

To disable the failing cpu, in this example, Node 0 CPU 4, at the tcsh/dsh prompt do the following:

```
ccmu up : clear 0 c4 : down
                ^  ^
                n  c
                o  p
                d  u
                e
```

Then run the test again.

6.18.1 Testing SPP1000's for PA7100 Problems (continued)

DATA CORRUPTION FAILURES

If data corruption failures are encountered and NO HPMC failures are detected, the test will run to completion with no additional user intervention required. See fail.examples for an example of a data corruption failure and NO HPMC failures.

NO FAILURES DETECTED

See fail.examples for an example of a test run with no failures.

5. When the test has been run to completion, with no HPMC failures, restore the original MU parameters with the following commands.
   "ccmu pull"
   "do_reset"

6. If you turned the OBP auto-reboot? flag to false, set it back to true at this time.

7. Boot SPP-UX and return the system to the customer.

DATA CORRUPTION FAILURES

If data corruption failures are encountered and NO HPMC failures are detected, the test will run to completion with no additional user intervention required. See fail.examples for an example of a data corruption failure and NO HPMC failures.

NO FAILURES DETECTED

See fail.examples for an example of a test run with no failures.

5. When the test has been run to completion, with no HPMC failures, restore the original MU parameters with the following commands.
   "ccmu pull"
   "do_reset"

6. If you turned the OBP auto-reboot? flag to false, set it back to true at this time.

7. Boot SPP-UX and return the system to the customer.


```
*** FAILURE EXAMPLES ***

HPMC FAILURES
-------------
********* Begin Testing 16 CPUS on COMPLEX_SN 65654

********* Running sppring Version

CONVEX Version Info:   0.0.72.80

********* beginning nominal clock/nominal power
Starting sppring at Thu Apr 27 10:34:05 1995
Doing sysreset.....Done.
Memory board available for Node 0 : 0 1 2 3
Memory board available for Node 1 : 0 1 2 3
Tchip available for Node 0 : 0 1 2 3 4 5 6 7
Slice available for Node 0 : 0 1 2 3
CMC DARK found on Node 0
Tchip available for Node 1 : 0 1 2 3 4 5 6 7
Slice available for Node 1 : 0 1 2 3
CMC DARK found on Node 1
Node 0 Tchip 0 Dcache 1024K Icache 1024K
Node 0 Tchip 1 Dcache 1024K Icache 1024K
Node 0 Tchip 2 Dcache 1024K Icache 1024K
Node 0 Tchip 3 Dcache 1024K Icache 1024K
Node 0 Tchip 4 Dcache 1024K Icache 1024K
Node 0 Tchip 5 Dcache 1024K Icache 1024K
Node 0 Tchip 6 Dcache 1024K Icache 1024K
Node 0 Tchip 7 Dcache 1024K Icache 1024K
Node 1 Tchip 0 Dcache 1024K Icache 1024K
Node 1 Tchip 1 Dcache 1024K Icache 1024K
Node 1 Tchip 2 Dcache 1024K Icache 1024K
Node 1 Tchip 3 Dcache 1024K Icache 1024K
Node 1 Tchip 4 Dcache 1024K Icache 1024K
Node 1 Tchip 5 Dcache 1024K Icache 1024K
Node 1 Tchip 6 Dcache 1024K Icache 1024K
Node 1 Tchip 7 Dcache 1024K Icache 1024K
        Subtest 5060 - HP Dcache Verification Test
Entry address : 0x18e8
Text address  : 0x1000
Text size     : 0x1a004
Text pointer  : 0x4000
Data address  : 0x21000
Data size     : 0x2000
Data pointer  : 0x1f000
BSS size      : 0x10c68
  failed
+++>  246
<Thu Apr 27 10:34:55 1995>  error:0x856b0564
sppring:0.0.72.80:util.c:128
ERROR: Received unexpected trap from Node 0 CPU  4
       Expected trap : 0xffffffff    Actual trap : 0x1
HPMC: No error entry found in HOURINI database.
****
```

6.18.1 Testing SPP1000's for PA7100 Problems (continued)

```
  +++>  119
  <Thu Apr 27 10:39:53 1995>  error:0x856b0558
  sppring:0.0.72.80:util.c:201
  ERROR: Timeout Node 0 CPU 4
  ****

  INITWHAT value for Node 0 : 0x5b00cfff
  INITWHAT value for Node 1 : 0x5b00cfff

  Closing all T-chip channels..... please wait.....
  +++>  196
  <Thu Apr 27 10:39:55 1995>  info:0x456b0406
  sppring:0.0.72.80:../main.c:63
  terminating - testing failed
  elapsed time:  05:50
  Terminating with 2 error at Thu Apr 27 10:39:55 1995


  DATA CORRUPTION FAILURES
  ------------------------

  ********* Begin Testing 16 CPUS

  ********* Running sppring Version

  CONVEX Version Info:   0.0.72.80
  .
  .

  ********* beginning nominal clock/upper   power
  Starting sppring at Thu Apr 27 10:36:16 1995
  Doing sysreset.....Done.
  Memory board available for Node 0 : 0 1 2 3
  Memory board available for Node 1 : 0 1 2 3
  Tchip available for Node 0 : 0 1 2 3 4 5 6 7
  Slice available for Node 0 : 0 1 2 3
  CMC DARK found on Node 0
  Tchip available for Node 1 : 0 1 2 3 4 5 6 7
  Slice available for Node 1 : 0 1 2 3
  CMC DARK found on Node 1
  Node 0 Tchip 0 Dcache 1024K Icache 1024K
  Node 0 Tchip 1 Dcache 1024K Icache 1024K
  Node 0 Tchip 2 Dcache 1024K Icache 1024K
  Node 0 Tchip 3 Dcache 1024K Icache 1024K
  Node 0 Tchip 4 Dcache 1024K Icache 1024K
  Node 0 Tchip 5 Dcache 1024K Icache 1024K
  Node 0 Tchip 6 Dcache 1024K Icache 1024K
  Node 0 Tchip 7 Dcache 1024K Icache 1024K
  Node 1 Tchip 0 Dcache 1024K Icache 1024K
  Node 1 Tchip 1 Dcache 1024K Icache 1024K
  Node 1 Tchip 2 Dcache 1024K Icache 1024K
  Node 1 Tchip 3 Dcache 1024K Icache 1024K
  Node 1 Tchip 4 Dcache 1024K Icache 1024K
```


6.18.1 Testing SPP1000's for PA7100 Problems (continued)

```
  Node 1 Tchip 5 Dcache 1024K Icache 1024K
  Node 1 Tchip 6 Dcache 1024K Icache 1024K
  Node 1 Tchip 7 Dcache 1024K Icache 1024K
          Subtest 5060 - HP Dcache Verification Test
  Entry address : 0x18e8
  Text address  : 0x1000
  Text size     : 0x1a004
  Text pointer  : 0x4000
  Data address  : 0x21000
  Data size     : 0x2000
  Data pointer  : 0x1f000
  BSS size      : 0x10c68
    failed
  +++>  559
  <Thu Apr 27 10:36:48 1995>  error:0x856b065f
  sppring:0.0.72.80:class5.c:321
  ERROR: Test fails on Node 0 CPU 7 with value of 0x00010001
         Bit 0 : no failure
         Bit 1 : no failure
         Bit 2 : no failure
         Bit 3 : no failure
         Bit 4 : < 2 percent total failures
         Bit 5 : no failure
         Bit 6 : no failure
         Bit 7 : no failure
         Bit 8 : no failure
         Bit 9 : no failure
         Bit 10 : no failure
         Bit 11 : no failure
         FP Failure : no failure
         Degree of Badness : 0x1 (0 = worst case)****

  +++>  559
  <Thu Apr 27 10:36:48 1995>  error:0x856b065f
  sppring:0.0.72.80:class5.c:321
  ERROR: Test fails on Node 1 CPU 3 with value of 0x00010005
         Bit 0 : no failure
         Bit 1 : no failure
         Bit 2 : no failure
         Bit 3 : no failure
         Bit 4 : < 2 percent total failures
         Bit 5 : no failure
         Bit 6 : no failure
         Bit 7 : no failure
         Bit 8 : no failure
         Bit 9 : no failure
         Bit 10 : no failure
         Bit 11 : no failure
         FP Failure : no failure
         Degree of Badness : 0x5 (0 = worst case)****
```

6.18.1 Testing SPP1000's for PA7100 Problems (continued)

```
  INITWHAT value for Node 0 : 0x5b00cfff
  INITWHAT value for Node 1 : 0x5b00cfff

  Closing all T-chip channels..... please wait......
  +++>  196
  <Thu Apr 27 10:36:52 1995>  info:0x456b0406
  sppring:0.0.72.80:../main.c:63
  terminating - testing failed
  elapsed time:  00:36
  Terminating with 2 error at Thu Apr 27 10:36:52 1995
  .
  ****

  ********* completed nominal clock/upper   power

  ********* Completed Testing 16 CPUS

  NO FAILURES DETECTED
  --------------------

  ********* Begin Testing 16 CPUS on COMPLEX_SN 65654

  ********* Running sppring Version

  CONVEX Version Info:   0.0.72.80

  ********* beginning nominal clock/nominal power
  Starting sppring at Thu Apr 27 10:34:05 1995
  Doing sysreset.....Done.
  Memory board available for Node 0 : 0 1 2 3
  Memory board available for Node 1 : 0 1 2 3
  Tchip available for Node 0 : 0 1 2 3 4 5 6 7
  Slice available for Node 0 : 0 1 2 3
  CMC DARK found on Node 0
  Tchip available for Node 1 : 0 1 2 3 4 5 6 7
  Slice available for Node 1 : 0 1 2 3
  CMC DARK found on Node 1
  Node 0 Tchip 0 Dcache 1024K Icache 1024K
  Node 0 Tchip 1 Dcache 1024K Icache 1024K
  Node 0 Tchip 2 Dcache 1024K Icache 1024K
  Node 0 Tchip 3 Dcache 1024K Icache 1024K
  Node 0 Tchip 4 Dcache 1024K Icache 1024K
  Node 0 Tchip 5 Dcache 1024K Icache 1024K
  Node 0 Tchip 6 Dcache 1024K Icache 1024K
  Node 0 Tchip 7 Dcache 1024K Icache 1024K
  Node 1 Tchip 0 Dcache 1024K Icache 1024K
  Node 1 Tchip 1 Dcache 1024K Icache 1024K
  Node 1 Tchip 2 Dcache 1024K Icache 1024K
  Node 1 Tchip 3 Dcache 1024K Icache 1024K
  Node 1 Tchip 4 Dcache 1024K Icache 1024K
  Node 1 Tchip 5 Dcache 1024K Icache 1024K
  Node 1 Tchip 6 Dcache 1024K Icache 1024K
  Node 1 Tchip 7 Dcache 1024K Icache 1024K
```


6.18.1 Testing SPP1000's for PA7100 Problems (continued)

```
       Subtest 5060 - HP Dcache Verification Test
  Entry address : 0x18e8
  Text address  : 0x1000
  Text size     : 0x1a004
  Text pointer  : 0x4000
  Data address  : 0x21000
  Data size     : 0x2000
  Data pointer  : 0x1f000
  BSS size      : 0x10c68
  0:00:25   passed
  INITWHAT value for Node 0 : 0x5b00cfff
  INITWHAT value for Node 1 : 0x5b00cfff

  Closing all T-chip channels..... please wait......
  +++>  192
  <Thu Apr 27 10:34:41 1995>  info:0x456b0405
  sppring:0.0.72.80:../main.c:71
  terminating - testing passed
  elapsed time:  00:36
  Terminating normally at Thu Apr 27 10:34:41 1995
  .
  ****

  ********* completed nominal clock/nominal power

  ********* beginning upper   clock/nominal power
  Starting sppring at Thu Apr 27 10:35:12 1995
  Doing sysreset.....Done.
  Memory board available for Node 0 : 0 1 2 3
  Memory board available for Node 1 : 0 1 2 3
  Tchip available for Node 0 : 0 1 2 3 4 5 6 7
  Slice available for Node 0 : 0 1 2 3
  CMC DARK found on Node 0
  Tchip available for Node 1 : 0 1 2 3 4 5 6 7
  Slice available for Node 1 : 0 1 2 3
  CMC DARK found on Node 1
  Node 0 Tchip 0 Dcache 1024K Icache 1024K
  Node 0 Tchip 1 Dcache 1024K Icache 1024K
  Node 0 Tchip 2 Dcache 1024K Icache 1024K
  Node 0 Tchip 3 Dcache 1024K Icache 1024K
  Node 0 Tchip 4 Dcache 1024K Icache 1024K
  Node 0 Tchip 5 Dcache 1024K Icache 1024K
  Node 0 Tchip 6 Dcache 1024K Icache 1024K
  Node 0 Tchip 7 Dcache 1024K Icache 1024K
  Node 1 Tchip 0 Dcache 1024K Icache 1024K
  Node 1 Tchip 1 Dcache 1024K Icache 1024K
  Node 1 Tchip 2 Dcache 1024K Icache 1024K
  Node 1 Tchip 3 Dcache 1024K Icache 1024K
  Node 1 Tchip 4 Dcache 1024K Icache 1024K
  Node 1 Tchip 5 Dcache 1024K Icache 1024K
  Node 1 Tchip 6 Dcache 1024K Icache 1024K
```

```
  Node 1 Tchip 7 Dcache 1024K Icache 1024K

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6.18.1 Testing SPP1000's for PA7100 Problems (continued)
------------------------------------------------------------

      Subtest 5060 - HP Dcache Verification Test
  Entry address : 0x18e8
  Text address  : 0x1000
  Text size     : 0x1a004
  Text pointer  : 0x4000
  Data address  : 0x21000
  Data size     : 0x2000
  Data pointer  : 0x1f000
  BSS size      : 0x10c68
  0:00:23   passed
  INITWHAT value for Node 0 : 0x5b00cfff
  INITWHAT value for Node 1 : 0x5b00cfff

  Closing all T-chip channels..... please wait......
  +++>  192
  <Thu Apr 27 10:35:45 1995>  info:0x456b0405
  sppring:0.0.72.80:../main.c:71
  terminating - testing passed
  elapsed time:  00:33
  Terminating normally at Thu Apr 27 10:35:45 1995
  .
  ****

  ********* completed upper   clock/nominal power

  ********* beginning nominal clock/upper   power
  Starting sppring at Thu Apr 27 10:36:16 1995
  Doing sysreset.....Done.
  Memory board available for Node 0 : 0 1 2 3
  Memory board available for Node 1 : 0 1 2 3
  Tchip available for Node 0 : 0 1 2 3 4 5 6 7
  Slice available for Node 0 : 0 1 2 3
  CMC DARK found on Node 0
  Tchip available for Node 1 : 0 1 2 3 4 5 6 7
  Slice available for Node 1 : 0 1 2 3
  CMC DARK found on Node 1
  Node 0 Tchip 0 Dcache 1024K Icache 1024K
  Node 0 Tchip 1 Dcache 1024K Icache 1024K
  Node 0 Tchip 2 Dcache 1024K Icache 1024K
  Node 0 Tchip 3 Dcache 1024K Icache 1024K
  Node 0 Tchip 4 Dcache 1024K Icache 1024K
  Node 0 Tchip 5 Dcache 1024K Icache 1024K
  Node 0 Tchip 6 Dcache 1024K Icache 1024K
  Node 0 Tchip 7 Dcache 1024K Icache 1024K
  Node 1 Tchip 0 Dcache 1024K Icache 1024K
  Node 1 Tchip 1 Dcache 1024K Icache 1024K
  Node 1 Tchip 2 Dcache 1024K Icache 1024K
  Node 1 Tchip 3 Dcache 1024K Icache 1024K
  Node 1 Tchip 4 Dcache 1024K Icache 1024K
  Node 1 Tchip 5 Dcache 1024K Icache 1024K
  Node 1 Tchip 6 Dcache 1024K Icache 1024K
  Node 1 Tchip 7 Dcache 1024K Icache 1024K

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6.18.1 Testing SPP1000's for PA7100 Problems (continued)
------------------------------------------------------------

      Subtest 5060 - HP Dcache Verification Test
  Entry address : 0x18e8
  Text address  : 0x1000
  Text size     : 0x1a004
  Text pointer  : 0x4000
  Data address  : 0x21000
  Data size     : 0x2000
  Data pointer  : 0x1f000
  BSS size      : 0x10c68
  0:00:25   passed
  INITWHAT value for Node 0 : 0x5b00cfff
  INITWHAT value for Node 1 : 0x5b00cfff

  Closing all T-chip channels..... please wait......
  +++>  196
  <Thu Apr 27 10:36:52 1995>  info:0x456b0406
  sppring:0.0.72.80:../main.c:63
  sppring:0.0.72.80:../main.c:71
  terminating - testing passed
  elapsed time:  00:33
  Terminating normally at Thu Apr 27 10:35:45 1995
  .
  ****

  ********* completed nominal clock/upper   power

  ********* beginning upper   clock/upper   power
  Starting sppring at Thu Apr 27 10:37:22 1995
  Doing sysreset.....Done.
  Memory board available for Node 0 : 0 1 2 3
  Memory board available for Node 1 : 0 1 2 3
  Tchip available for Node 0 : 0 1 2 3 4 5 6 7
  Slice available for Node 0 : 0 1 2 3
  CMC DARK found on Node 0
  Tchip available for Node 1 : 0 1 2 3 4 5 6 7
  Slice available for Node 1 : 0 1 2 3
  CMC DARK found on Node 1
  Node 0 Tchip 0 Dcache 1024K Icache 1024K
  Node 0 Tchip 1 Dcache 1024K Icache 1024K
  Node 0 Tchip 2 Dcache 1024K Icache 1024K
  Node 0 Tchip 3 Dcache 1024K Icache 1024K
  Node 0 Tchip 4 Dcache 1024K Icache 1024K
  Node 0 Tchip 5 Dcache 1024K Icache 1024K
  Node 0 Tchip 6 Dcache 1024K Icache 1024K
  Node 0 Tchip 7 Dcache 1024K Icache 1024K
  Node 1 Tchip 0 Dcache 1024K Icache 1024K
  Node 1 Tchip 1 Dcache 1024K Icache 1024K
  Node 1 Tchip 2 Dcache 1024K Icache 1024K
  Node 1 Tchip 3 Dcache 1024K Icache 1024K
```

```
  Node 1 Tchip 4 Dcache 1024K Icache 1024K
  Node 1 Tchip 5 Dcache 1024K Icache 1024K
  Node 1 Tchip 6 Dcache 1024K Icache 1024K
  Node 1 Tchip 7 Dcache 1024K Icache 1024K
```


6.18.1 Testing SPP1000's for PA7100 Problems (continued)

```
      Subtest 5060 - HP Dcache Verification Test
  Entry address : 0x18e8
  Text address  : 0x1000
  Text size     : 0x1a004
  Text pointer  : 0x4000
  Data address  : 0x21000
  Data size     : 0x2000
  Data pointer  : 0x1f000
  BSS size      : 0x10c68
  0:00:25   passed
  INITWHAT value for Node 0 : 0x5b00cfff
  INITWHAT value for Node 1 : 0x5b00cfff

  Closing all T-chip channels..... please wait......
  +++>  196
  <Thu Apr 27 10:38:02 1995>  info:0x456b0406
  sppring:0.0.72.80:../main.c:71
  terminating - testing passed
  elapsed time:  00:33
  Terminating normally at Thu Apr 27 10:35:45 1995
  .
  ****

  ********* completed upper   clock/upper   power

  ********* cop information

  COMPLEX_SN 65654

  0    A0   0  TCHP  000001     1111451
  0    B0   1  TCHP  000001     1112529
  0    A1   2  TCHP  000001     1112527
  0    B1   3  TCHP  000001     1112528
  0    A2   4  TCHP  000001     1112865
  0    B2   5  TCHP  000001     1112864
  0    A3   6  TCHP  000001     1112862
  0    B3   7  TCHP  000001     1112860
  1    A0   0  TCHP  000001     1111297
  1    B0   1  TCHP  000001     1112858
  1    A1   2  TCHP  000001     1111287
  1    B1   3  TCHP  000001     1112861
  1    A2   4  TCHP  000001     1111295
  1    B2   5  TCHP  000001     1112859
  1    A3   6  TCHP  000001     1111285
  1    B3   7  TCHP  000001     1112863

  ********* Completed Testing 16 CPUS on COMPLEX_SN 65654
```


6.18.2 C3800/QSC and Diag v4.2

The respun QSC, part number 410-002447, was inadvertantly left out of the database, in the 4.2 Diagnostic release. The original 1447 board was included, but not the released QSC.

All other necessary changes have been made, so the solution to this oversight is simple and straight forward:

1) Add the following entry to /diag/db/part_numbers:

```
       410-002447/qsc/1&1:C-B,ZZ-ZZ;&
```

2) Execute the add_parts utility. If this is not done, the new entry will not be added to the CDB, until the next reboot of the SPU.

3) Continue with installation of the QSC

6.18.3 QSC and the Plsi Explanation

The QSC was designed so that most board modifications can be accomplished by downloading a new database into the plsi array, located on the QSC.

This new database may be received, by the field, in one of two ways. In most cases, a new install format tape will be received, to be installed on the system. In some critical, or test situations, it may be necessary to ftp the database directly onto the system.

The database will be moved into one of two directories, depending on the type of system involved. On C38/C4600 systems, then database will be moved into /diag/db. On C2's and C3400's it will be necessary to move the database into /mnt/usr/lib/plsi.

To install the database and use it, the follwoing procedure will be used. In the case of an install tape, most of this will be accomplished by the install script:

1) Take system to the SPU level.

2) Copy the file to the spu, e.g.:

   cd /mnt/usr/lib/plsi, or /diag/db
   cp qsc_plsi.db qsc_plsi.db.1.0 (on subsequent releases, this will not be necessary)
   mv the new qsc_plsi.db.xx, to this directory.

3) In cases where the database is provided by a means other than an install tape, checksums will be provided to verify the database. The verification will be accomplished by; qsc_ldplsi -i. An example of the output can be seen below:

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6.18.3 C3800/QSC and Diag v4.2 (continued)

---

verify that the output looks like this:

```
pLSI database rev 1.X
181_008228 -- Checksum = 0xdbbd, CREATED DATE:  Wed Apr 19 11:05:09 1995
181_008231 -- Checksum = 0x63e8, CREATED DATE:  Mon Dec 12 09:52:26 1994
181_008232 -- Checksum = 0xa3bc, CREATED DATE:  Thu Dec 29 10:37:48 1994
181_008250 -- Checksum = 0xbaae, CREATED DATE:  Tue Nov 29 11:26:55 1994
181_008251 -- Checksum = 0x4ad, CREATED DATE:  Fri Dec 16 15:05:58 1994
181_008252 -- Checksum = 0x863d, CREATED DATE:  Fri Mar  3 16:58:11 1995
181_008245 -- Checksum = 0x55d6, CREATED DATE:  Wed Mar  8 20:02:25 1995
181_008242 -- Checksum = 0xcb82, CREATED DATE:  Fri Feb  3 15:34:55 1995
181_008244 -- Checksum = 0x17f7, CREATED DATE:  Fri Feb  3 15:38:43 1995
```

4) In order to download the database, to the board, the following must be done. It should be understood that this cannot be accomplished on a system at multiuser.

```
qsc_ldplsi -c ## -l 1032
qsc_ldplsi -c ## -l 2032  <where ## is slot number of the QSC>
```

5) To verify the load was successful:

```
qsc_ldplsi -c ## -C hw -p 1032
qsc_ldplsi -c ## -C hw -p 2032
```

6) Reboot

Examples and available switches for use with the qsc_ldplsi utility are shown below:

Comman line options:

```
-c <ccu>
-b                          // Build new database
-r <major><minor>           // Revision of database
-i                          // List rev and checksums of database
-v [1032] [2032]            // select plsi group to verify
-l [1032] [2032]            // select plsi group to download
-C [hw] [db]                // Verify checksum of hw, or database
-p [1032] [2032]            // Use when -l, or -v haven't been used
-d <directory>              // Directory of database and/or JEDEC's. Used
                               during build.
```

Examples:

```
qsc_ldplsi -b /foo/jedecdir -r 0.9    // Build database
qsc_ldplsi -v 1 -c 0                  // Verify 1032's of ccu0
qsc_ldplsi -l 2 -c 0                  // download 2032's of CCu 0
qsc_ldplsi -C hw -c 0 -p 2            // Verify checksum of 2032's or ccu0
qsc_ldplsi -C db                      // Verify checksum of database
qsc_ldplsi -C hw -v 2 -c 0            // Verifyy and perform checksum
qsc_ldplsi -i                         // What's in database
```

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6.18.4 C4 Errintd Hangs

A new Errintd problem has been discovered with the C4600. This problem does not, apparently, involve a failed assisted, or soft processor error.

As with the previous recommendation, attempt to find evidence of an assisted, or processor soft error, in the asst_log, or soft_log. It may also be noted in the errlog, if an assisted error. If this evidence exists, it may still be possible to kill errintd and clear the problem. If no evidence of one of these events exists, then it is likely the new condition. This new condition is explained below:

It appears that, for some unknown reason, it is possible for errintd and cdbserver begin to spin and assume all available cpu time, on the SPU. This results in a very slow JP, which will ultimately require a reboot to clear.

In order to reboot the system it will be necessary to kill the errintd process. It will not be possible to clear the errintd state, until the system is brought to the SPU. Until this happens, the new errintd process will start and achieve the same state.

If the errintd process is not restarted, before attempting the reboot, the following failure will be seen during the boot:

```
[CPU00@09:39:11] rebooting ConvexOS
Cleaning up SPU processes...

Calling change_errintd_options
localhost: RPC: Timed out
change_errintd_options() failed
start_errintd: Error 0
```

This problem is very intermittent and has only been seen a few times.

The important thing to remember is that in most cases, it is possible perform a planned reboot, if the condition is caught soon enough.

6.18.5 Datatower Diag incompatibility with Screen Enhancer

It has been discovered that the cas_diags, for the Datatower and the Toshiba, Ultra screen enhancer, are incompatible, on the same laptop.

A simple workaround, for this incompatibility, is to remove the entry LH C:\DOS\ULTRA.COM, from the file autoexec.bat.

To be able to run Ultra with other applications, it would be necessary

to reenter the abive line. As this would be quite awkward, it is recommended that two different autoexec.bat files be used, so it will be possible to move back and forth.

Thanks to Marc Morin, for this tip.

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Contents of this issue:

1. SPP Diags 3.0 hard_logger Bug.
2. Diag Failures with 4GB Drive on SPP.

6.20.1 SPP Diags 3.0 hard_logger Bug

A bug has been found in the 3.0 hard_logger.
This bugs prevents scanning slice 3, in the case of a hard error.
A fixed version of hard_logger is now available.
All SPP's(1000's and 1200's), running Diags 3.0, should install this fixed version.
The new hard_logger is located in /common/tachwbul/hard_logger.3.1.

*** Installation ***

Retrieve /common/tachwbul/hard_logger.3.1

As sppuser:
Place hard_logger.3.1 in /spp/scripts/hard_logger.3.1
cp -p /spp/scripts/hard_logger /spp/scripts/hard_logger.3.0
chmod 754 /spp/scripts/hard_logger
cp /spp/scripts/hard_logger.3.1 /spp/scripts/hard_logger
chmod 554 spp/scripts/hard_logger
verify owner, group and permissions -r-xr-xr-- 1 sppuser sppuser

Installation is complete.

6.20.2 Diag Failures with 4GB Drive on SPP

It has been discovered that iod will fail, at different subtests, when run on a 4GB drive. The failure exhibited will be a "scsi_exec" failure.

This problem should be resolved in the next teststation diagnostic release. Which will be greater than 3.0 and released by the end of May.

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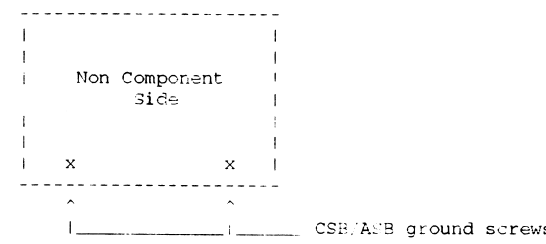
Contents of this issue:

1. SPP Gate Array Torque and CSB/ASB Ground Check
2. Running Sppring Before and After Upgrading SPP-UX
3. Adding 2nd SCSI to Landmark(SIOP1)
4. CONVEX Quick PM Checklist
5. MU/SCI Parameter change for V3.1 DIAGS

6.23.1 SPP Gate Array Torque and CSB/ASB Ground Check

It is recommended to verify the SPP gate arrays are torqued to 5 in/lbs during system installation. This should be re-checked, during PM, at 90 day intervals. Additionally the CSB/ASB ground screws should be checked for a secure fit. There is no specific torque spec for these screws.

Remember to torque the gate arrays in an X pattern.



6.23.2 Running Sppring Before and After Upgrading SPP-UX

Many times when SPP-UX and teststation diags are upgraded, ccmu parameters are changed to a new value. Sometimes these new parameter values will bring an existing hardware problem to light. Therefore it is recommended to run sppring -s 9480-9590 and sppring -c 10 before and after upgrading SPP-UX or the teststation diags. This will give us a point of reference in the event of problems arising after a software upgrade.

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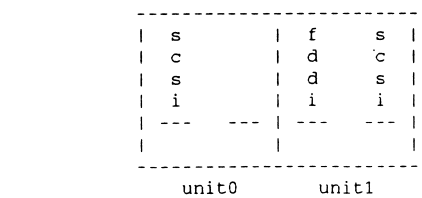
6.23.3 Adding 2nd SCSI to Landmark(SIOP1)

The Landmark card is basically split into 2 logical units. Unit 0 and Unit 1. The 1st SCSI controller is always placed on unit 0 sbus 0. The 2nd SCSI controller should always be placed on unit 1. If there is a FDDI controller it will be placed on unit 1 sbus0 so a 2nd SCSI would be placed on unit 1 sbus 1.

This will avoid potential SCSI conflicts and possibly improve performance.

Here is how a Landmark card with 2 SCSIs and 1 FDDI should be configured.



6.23.4 CONVEX Quick PM Checklist

It is understood that it is not feasible to accomplish specific PM visits on sites, due to customer and time pressures. Because of this, it is recommended that the following checklist be accomplished on routine or corrective maintenance visits, to sites.

It is requested that the acomplishment of this PM checklist be annotated on all PR's resulting in a site visit.

I. All Systems:

1) Check errlog for unknown system and peripheral errors. Take corrective action as necessary.

2) Check correct power supply voltages on-line.
   a) On C1/C2/C34 class systems, use margin command, to obtain operating voltages.
   b) On C38/C46 class systems, use xpowermon.
   c) On SPP, use pce_util.

3) Visually inspect all external filters and clean if dirty.

4) Check soft_log for excessive memory soft errors.
   a) For C38/C46 systems, this includes IA and processor soft errors.
   b) No soft_log on SPP systems.

5) Verify tape drives being cleaned properly, by customer.

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6.23.4 CONVEX Quick PM Checklist (continued)

6) Visual Inspection.

7) Consult with customer on unreported problems.

II. C3800's and C4600's

1) Check event_log, over last week, for signs of environmental errors.

2) check /var/adm/messages file, on SPU, for signs of SPU async errors.

3) On C4600's check asst_log file for signs of assisted errors and slip if necessary.

III. SPP

1) Check /usr/adm/syslog file, on teststation, for signs of teststation problems.

2) Check fans and environmental parameters with pce_util

6.23.5 MU/SCI Parameter change for V3.1 DIAGS

It is recommended that the MU parameter, SCI_SYNC_INTERVAL, be changed, from a value of 0x00000400 to 0x00004000, when upgrading to v3.1 Diagnostics. It was intended that this be modified by the auto command, in ccmu, but will not change if a value exists. For this reason, it is necessary to accomplish this manually, for each node.

This parameter reduces the number of syncs sent between packets.

This change can be accomplished under ccmu, with the put command, by ccmu up : put SCI_SYNC_INTERVAL 0x00004000 : down.

Contents of this issue:
1. ER-90/FileServ Error
2. SPP Multi-node Debug Hints

6.25.1 ER-90/FileServ Error

If the following error has been observed:

"Jun 16 07:19:01 F0039:11:<00000>:msa2tsc374:fs_fmover(13833): 1 Operational Thresholds were exceeded for 'DESTINATION' device /dev/er90/s0, media 0000023"

The following may be of interest.

In short this type of error is trying to tell us that we have a problem with a drive or tape.

Thresholds are setup whereby errors reported by the drive will add to a count, and the errors can be re-reads or re-writes. If errors continue then a threshold is exceeded and the drive is removed from operation.

When an error is detected during the drives operation, the threshold count is increased. It now takes some number of "successful" actions, either reads or writes, before the threshold count is reduced. One good read or write does not wipe out one bad one.

Two commands will list the threshold values:-

For FileServ 2.2 "fstsdump" and "fstsrpt"
For FileServ 3.0 "fsmederr" and "fsmederrparms"

There are no hard and fast rules about threshold values, you just have to look at the various ones listed to see if one is out of line with the rest.

example:-

```
Play_Head1_Error_Count_Write_Operations: 131402

Play_Head2_Error_Count_Write_Operations: 21049

Play_Head3_Error_Count_Write_Operations: 22133

Play_Head4_Error_Count_Write_Operations: 10623
```

This portion of a threshold listing shows that Head 1 values are much higher than the rest, and could be the cause of the failure.

The correct action now would be to use the diagnostic pc to run further tests on this drive.

6.25.2 SPP Multi-Node Debug Hints

I. The Event_Log and the System Console

The first things to examine are the system console and the event_log. The system console will have information printed by the OS in the event of an HPMC or an assert. This information will include the node and cpu which has taken the HPMC.

```
[2:1] HPMC: Received HOURINI error response. (bit 15)
[2:1] isr=0x00000000 ior=0xffe10e14 iir=0x4b9c0000
[2:1] iisq_head=0x00000000 iioq_head=0x001f4570
[2:1] iisq_tail=0x00000000 iioq_tail=0x001f4574
[2:1] HPMC: Error found in node 2, cpu 1, HOURINI database entry 0:
[2:1] major_request: BASIC (0x0), minor_request: DFLUSHG (0x6)
[2:1] route: 0x8, p0: 0x2310, p1: 0x2f0, p2: 0x0
[2:1] last: 0x2  msg_index: 0x0
[2:1] parity_word_0: 0x5, parity_word_1: 0x1
[2:1] error: 0x1, valid: 0x1, rsb: 0x0, time_out_cntr: 0x0
[2:1] inv_cntr: 0x0, byte_write_data: 0xf9
[2:1] major_response: BASIC (0x0), minor_response: DFLUSHG (0x6)
[2:1] source: 0x1, tid: 0x0
[2:1] chip_id: CCMC 0 (0x8), class: ERR_CHIP (0x1)
[2:1] type: ERR_RES (0x1), error_code: RQ_RESP_ERR (0x107)
```

The source of this message was processor 1 on node 2. The message indicates that the processor was HPMC'd because it received an error response for one of its outstanding requests. This is indicated by a couple of lines in the console output.

```
[2:1] HPMC: Received HOURINI error response. (bit 15)
```

Bit 15 of the exc_cause register in the processor agent is set when an error response is received.

```
[2:1] chip_id: CCMC 0 (0x8), class: ERR_CHIP (0x1)
[2:1] type: ERR_RES (0x1), error_code: RQ_RESP_ERR (0x107)
```

The id of the chip which detected (or relayed) the error is indicated in the 2 lines above. This error was detected by CCMC 0. The fact that the error_code field has a 1 in the MS hex digit implies that the error was in fact detected by the SCI chip and returned to the CCMC. The LS byte of the error_code field gives the actual error code that was returned. A table of the common error codes follows. A complete list of these error codes is available in the gate array specifications (CCMC and SCI).

6.25.2 SPP Multi-Node Debug Hints (continued)

error_code	source	description

0x82	cmc	Non-coherent access to coherent space. Usually indicates a SW problem.
0x87	cmc	Mem aliasing error. indicates a problem with a BDT mapping. Usually indicates a SW problem
0x88	cmc	Virtual index error. Processor accessed an encached line with a different virtual index. Usually indicates a SW problem
0x106	sci	No Echo and no resp recvd form target node. SCI request was dropped before getting to target node.
0x107	sci	No response rcvd. The request was received by the target node but was never served.
0x171	sci	External device timeout. The request was deleivered to the target node, made it to the CMC and never got a response. This error is seen many times when a hard error has been detected on the target node (clocks are stopped on the target).

In additon to the system console, HPMC's usually leave a footprint in the event_log. The information content is identical to that on the console, just in a diferent format.

```
<Wed May  3 22:37:34 1995>  error:0x82563fff
<OS>:0.0.0.0:<src ref>:2053744
node: 0x4 (4)
HPMC, node 4, CPU 1.  HOURINI entry 2.
EXC_CAUSE bit 15: Received HOURINI error response.
0x208006b0 0x55f9ae00 0x20800002 0x55f9a00d 0x8000300 0x8000000 0x0 0x80aa771
```

Here the last 9 bits of the last line of the event_log message gives the error code field described above. In this case it was a 0x171 error (External Device Timeout).

In addition to the HPMC info, hard errors are reported in the event_log. When a hard error is reported the hard_logger tries to interrogate the system to print useful error information to the event_log. Below is some sample hard_logger output.

```
<Wed May  3 22:37:59 1995>  error:0x856e4f02
log_event:3.0.0.0:../log_event.c:96
-------------------------------------------------------------------------------
 Hard error occured at : Wed May  3 22:37:45 MEST 1995
 NODE = 4 First Hard Error = 0001 Hard Error = 0001  Hard Error Mask = 1fff
-------------------------------------------------------------------------------
pce_util:   3.0 (Fri Mar 24 22:00:48 1995)

                node: 0x4 (4)

       status    description   state    current
       ------    -----------   -----    -------
       disabled  clocks        normal   free running
       on        -4.5 VEE_CLK  unknown  -4.506
       on        -3.1 VHE_HP   unknown  -3.100
```


6.25.2 SPP Multi-Node Debug Hints (continued)

The important stuff from this message is contained in the banner. It shows which node has pulled the hard error, which chip pulled the first hard error and all of the chips which subsequently pulled hard error. The fields are vectors with each bit representing a particular chip. Below is the bit definition of the vectors.

```
  0 -  19  20           23   24          27  28          31
  XXX MAUI IO1 IO0 XB-S XB-Q AG3 AG2 AG1 AG0 MC3 MC2 MC1 MC0

  IO0- I/O Unit 0
  IO1- I/O Unit 1
  XB-Q - Request Xbar
  XB-S - Response Xbar
  AG(0-3) - Processor Agent CPA
  MC(0-3) - CMC
```

The error listing from above indicates that the first hard error was pulled by CMC0 (First Hard Error = 0001). This was also the only hard error pulled in the node (Hard Error = 0001).

Usually accompanying this output in the event_log is a report from the hard_logger which formats raw error info from the chip which reported the error. An example of this output appears below.

```
<Wed May  3 22:37:58 1995>  error:0x856e062c
log_event:3.0.0.0:../log_event.c:96
-------------------------------------------------------------------------------
 NODE 0 CMC 2 detected a not_owner_err Coherency error

 Port = 2#101
-------------------------------------------------------------------------------
  --- RQI view of flow ---
      Access Type  = AT_LOCAL_MEM
      Major Type   = CopyOut (05)      Minor Type   =   (0)
      Addr(36 bit) = 0x0000fea80
      Src          = 01                TID (short)  = 03
      Tgt   Mem Sz = 3
      Buff Blk     = 0
      Buff Need    = 0
      Resend Queue = 0
      Old Tag      = 0x0000000000000000

              SBDT    PURGE_PRIV      TIME_OUT
              ------------------------------
               0      1               0
```


6.25.2 SPP Multi-Node Debug Hints (continued)

Here CMC2 on node 0 is reporting a not_owner error. This error indicates that a CopyOut has arrived at memory (the CMC) from a processor which is not marked as the owner of the line in the cache tags. This condition implies a coherency protocol error. Usually however this error results from the way the system handled a previous

HPMC to that processor. If this error is seen in the event_log it is a good bet that the actual problem occurred a while back (the HPMC) and that has finally resulted in a failure.

Several hard error conditions which are detected by the CMC fall into this category. The most common of these are the rqi_miss_err and the fl_rp_err. The rqi_miss_err is again a problem that happens subsequent to the reception of an HPMC (due to an sci timeout) by a processor. The fl_rp error occurs when EITHER the CMC receives an error response from SCI during a cache rollout operation or (and much less likely) we encounter a multi-bit ecc error when reading the flush data from memory. The format for these errors is very similar to that of the not_owner_err above.

The other important piece of information in the event_log is the message traffic generated by OD_SPIN_INV cleanup. The OD_SPIN_INV problem is a system problem which we have worked around using MU FW and OS support. Without going into the details of the algorithm, the messages indicate that a node has detected and is trying to clean up an OD_SPIN_INV problem. It is important to note that MANY problems can masquerade as the OD_SPIN problem and that seeing these messages in the event_log may not be an accurate indication of this type of problem. There are several types of messages that are associated with OD_SPIN cleanup. Some examples are shown below.

```
<Wed May  3 22:37:40 1995>  warning:0x62562000
<OS>:0.0.0.0:<src ref>:2113600
node: 0x1 (1)
Node 1,CPU 1, file ../../mpp1/sci_od_spin_invalid.c,line190:Detected request
for SCI OD_SPIN_INVALID cleanup
****
```

The above message is printed by the OS when it received a request from the MU to begin an OD_SPIN cleanup on node 1. The node which detects the problem will make one of these requests to EACH of the other nodes. So one of these messages will be seen for every node except the one which detected a problem.

When the node finishes the cleanup operation a message, similar to below, will be printed in the event_log.

```
<Wed May  3 22:37:51 1995>  warning:0x62562000
<OS>:0.0.0.0:<src ref>:2113504
node: 0x1 (1)
Node 1, CPU 1, file ../../mpp1/sci_od_spin_invalid.c, line 312: Successfully
completed SCI OD_SPIN_INVALID recovery for node 0x0, ring 0x2 elapsed time 7
seconds and 37038 microseconds
****
```


6.25.2 SPP Multi-Node Debug Hints (continued)

Again this will be printed by (complex_size - 1) nodes for each occurrence of the problem. The bottom line here is that you will see a lot of these messages in the event_log and that this does not indicate that you are seeing a different problem each time that one appears.

II. Debugging a Massive System failure

As mentioned in the section above when one of the SCI timeout errors (or any other error resulting in an HPMC) occur the system will typically crash soon thereafter. These types of crashes usually end up with most of the nodes pulling hard errors or with the OS panicing. These types of crashes are very messy and very difficult to debug.

Probably the best thing to do is just to take a scan dump of the system. This is done by running the dump_all script in the /spp/scripts/cpa directory on the test station. Redirect the output to a file on the teststation. We typically use the /tmp directory. The syntax looks like this:

```
dump_all <node_num_list> > file
```

Another important thing to do is to save any console information regarding HPMC's or panics into a file. Pertinent parts of the event_log can also be saved to a file.

The dump file can be analyzed using various formatting scripts to see what the state of some of the more important machines inside the arrays were doing when they were dumped. In a train wreck type crash this information is often not very useful. But it is possible to get an idea of what some of the HW was doing. More details on looking at scan dumps will be included in a later mail message. For now you should probably contact the TAC and let them know that you have a dump for someone to look at. Any information that can be learned from looking at the event_log would also be helpful.

The next thing to do after dumping the node is to try to verify the integrity of the HW in the system. The best way to do that is using the sppring diagnostics. If you have recently replaced any HW or moved chips around it is also a good idea to run CST.

The sppring diagnostics are broken up into a dozen or so classes. The most important classes that you can run when trying to verify multi-node system operation are the classes 9 and 10. These dignostics concentrate on stressing the multi-node data paths and the coherency handling logic in the CMC and SCI arrays. The class 9 diags attempt to run the DRAM tests (class 3) over the SCI ring to the local nodes nearest neighbor. This class of tests is divided to test each ring seperately and then all of the rings together. The breakdown of the tests is as follows:

6.25.2 SPP Multi-Node Debug Hints (continued)

```
9000-9110 Ring 0
9120-9230 Ring 1
9240-9350 Ring 2
9360-9470 Ring 3
9480-9590 All Rings
```

If a specific ring is suspected, it ispossible to execute on those subtests that stress that ring. At minimum, though, it is recommended running the 9480-9590 subtests once.

```
ts> sppring  -s 9480-9590
```

The class 10 diagnostics try to stress the internode coherency logic. There are, again, over a dozen subtests which make up the class 10 tests suite. It is recommended running class 10 tests, looping on the 10070 test for at least 5 iterations. A problem exists with looping on the 10070 test on systems with SCAM boards. The diagnostic may fail intermittently. To work resolve this issue, it is possible to reconfigure the sync_interval parameter using ccmu. The parameter should be set to 0x4000. This reduces the chance of hitting the problem but does not totally eliminate it. Systems with SCI3 arrays should not see this problem.

The SCI_SYNC_INTERVAL parameter should have been modified on all systems running 3.0.4 OS. An example of the change is shown below:

```
ccmu> pull
ccmu> up
ccmu> put sci_sync_interval 0x4000
ccmu> down
ccmu> push
ccmu> quit

ts> do_reset
ts> sppring -lt 5 -s 10070
```

If the diags fail then repeat the process targeting particular slices to try to isolate the bad components. The deconfiguration of slices can be accomplished by using either xconfig or ccmu. Continue narrowing the scope of the test until the bad component can be isolated. A more detailed methodology for debugging systems which are failing diags will be sent in a subsequent Tech Bulletin.

If diagnostics pass then it is best to disable the SCI and CPA timeouts and reboot the system. With these timeouts disabled the machine will hang instead of crashing in such a manner, as to reduce the ability to debug it. This will result in a system hang, thus preserving the necessary system state. The timeouts can be disabled. as shown below:

6.25.2 SPP Multi-Node Debug Hints (continued)

```
ccmu> pull
ccmu> up
ccmu> put sci_split_timeout 0
ccmu> put cpa_pmon_control 0
ccmu> down
ccmu> push

do_reset
```

A do_reset is necessary to download the newly entered parameters. After this, a reboot is required to enable these parameters. wait. It is a little more difficult to tell when the system is down with the timeouts turned off. The lcd displays, on the cabinet, can be examined, for indications. A hung system will often have "lost heartbeat". Instead of displaying the alternating * and + symbols, the hung processor(s) will either be static or displaying a "_" character. A hung system may or may not be pingable, so using ping as a method of determining system health is not reliable. Testin for a login prompt, on the console should yield no response, thus confirming a hung state.

III. Debugging System Hangs.

When a system hang is detected it is important to determine if any of the SCI rings are hung. The best way to do this is to run the verify_rings script in the /spp/scripts directory on the teststation. This script will try to read a register in each of the SCI chips in the complex. If this script terminates abnormally (i.e with xbar or maui timeouts) then one or more of the rings is hung.

IIIa. Ring Hangs

In the case of a ring hang the dump_all script, in /spp/scripts/cpa, will have to be executed.To run, redirect the output to a file on the teststation. The /tmp directory is recommended for this. Saving pertinent console and event_log data is very important (probably won't be much in a hang). Another necessary piece of information to note is the node/cpu's which appear to be hung.

```
ts> dump_all <node_list> > <dump_file>
```

After the dump completes, Two scripts exist to search the dump output for known signatures of existing bugs. The first script, located in /spp/scripts/cpa, is cmp_chk.

```
cmp_chk <node> <slice> [s <dump>]
```

Execute the script on every slice of the node that appeared to be hung. The script will search the dump file and determine if a known bug has been encountered. The other script is in /spp/scripts/cmc and is called plr_hang. The syntax for the command is as follows.

```
plr_hang <node> <slice> [s <dump>]
```


6.25.2 SPP Multi-Node Debug Hints (continued)

Again, run the script over every ring in the hung node. This script will look through the dump and determine if this bug is the cause.

Unfortunately, the problems that are found by these scripts do not, at this time, have a work around. It is believed that the occurrence of these problems should be very rare in the field.

In either case forward the failure information and the dump file to the

tachwsup alias.

At this point diagnostics has been executed on a previous crash and there is reason to believe that it will not uncover a problem. Still if the frequency of crashes on the system is high or if it is increasing then running the diags as described above may be a good idea after a crash.

After running the diags (and assuming that nothing is found) go ahead and reboot the system. Leave the timeouts turned off.

IIIb. Rings OK

If the rings do not appear to be hung then leave the system running (hanging?) and contact the TAC for someone to examine the system. If this is not practical then try the following:

A set of scripts exists on the teststation in the /spp/scripts directory called toc and pim. These scripts are used to get the internal register values of a stuck tchip. Before running the scripts make sure to take note of which procs/nodes seem to have lost heartbeat. This information will be useful for the people looking into the problem. Also include a brief update on the state of the led's with output of the scripts.

Another helpful scropt, m_hdb_display, is in /spp/scripts/cpa.

The current dates of the scripts are as follow:

```
# $CHeader: toc 1.2 95/05/25 15:33:58 $
# $CHeader: pim 1.2 95/04/10 09:33:00 $
# $CHeader: m_hdb_display 1.4 95/05/25 15:32:24 $
```

These versions can be found in 3.1 diagnostc release.

toc

This script should be executed forst.

This will cause the toc to be sent to all of the cpus in the complex. A message will be seen that will indicate the system will crash if executed and request verification. Answer yes. The toc script should execute and return to the teststation prompt.

pim <node> <cpu>

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6.25.2 SPP Multi-Node Debug Hints (continued)

This script should be executed next. It is necessary to execute the script for each processor in the failed node, unless the failed processor is known.

The pim script will output the register contents and the Hourini database to the window. Redirecting the output to a file does not seem to work correctly, but you can capture the output in a file directly by doing the following:

Press cntrl and left mouse button.
Select "Log to File".
Run the scripts.
Press cntrl and left mouse button.
De-Select "Log to File".

The output should be in the home directory as XtermLog.?????. For example, if it was executed in sppuser, the file would be /users/sppuser/XtermLog.?????.

Once all cpu's have been pim'ed in the complex, the file hould be forwarded to the TAC. Be sure to indicate which version of the OS was running, at the time of the crash, along with which nodes/procs were believed to be hung. The TAC will forward this info to someone for analysis.

After the information has been collected, return the system to the customer, leaving the timeouts disabled.

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Contents of this issue:

1. SPP1200 Power Up Problem.
2. SPP1200 Primary Loader Bug.
3. SCSI Tape Addressing.
4. Exabyte Tape Drives.
5. SPP1000/1200 "Timeout waiting on node communication".
6. Convex Press I/O Web Announcement.
7. QSC Released Product.
8. C-Series Scsiutil Supports Disk Firmware Download.

6.26.1 SPP1200 Power Up Problem.

The following is ONLY applicable to SPP 1200 systems.....
Machines shipping this quarter WILL have these "features".

If you power down the system with the OBP bit set in 'initwhat' (bit 23), you will get a MU bus error on power up. All SPP1200 machines shipped in Q2 will have this problem. If you see this happen, you will have to go into ccmu and reset 'initwhat' to disable OBP.

```
sppuser> ccmu
ccmu> up
ccmu> put initwhat 0x5980cfff  (example for GSM machine)
ccmu> down
ccmu> push
ccmu> quit
sppuser> do_reset
sppuser> poe_util -p off
```

You will then have to power cycle the SPP by using the switch on the left front of the Exemplar cabinet . Wait about 5-10 seconds and flip the switch back on. When the database generation is complete, you need to go back and re-enable the OBP bit.

```
sppuser> ccmu
ccmu> up
ccmu> put initwhat 0x5980cfff  (example for GSM machine)
ccmu> down
ccmu> push
ccmu> quit
sppuser> do_reset
```

After about 45 seconds, you should have your OBP console window.
At the 'ok' prompt you can now boot.

```
ok> boot
```

This problem will be fixed in the next release.

6.26.2 SPP1200 Primary Loader Bug.

'cputest' will not work on the 1200 system with the version of the primary loader on the 3.0.4 release tape. The "fixed" version of the primary loader is currently not available. SPP1200 systems shipped in Q2 will have this problem. This will be fixed in the next release. If you need to run 'cputest' on a customer's system, please contact the TACHWSUP.

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6.26.3 SCSI Tape Addressing.

It is now possible to see scsi errors with the following form.

```
[CCUxx@11:31:50]  scsi_tape(1,2,0,3)dev open(0x15) etc, etc, etc.
 -----                        - - - -
   |                          | | | |
   >>>> VIOP number           | | | >>>> subunit address
        (CCUxx)               | | |
                              | | >>>>>> unit address
                              | |
                              | >>>>>>>> VME slot number
                              |
                              >>>>>>>>>> VME port (0 or 1 for VME0 VME1)
```

The "unit address" is the address that is set in the drive.
The "subunit address" in most cases is always "0". The exception is when you have more than one Fujitsu 3480 formatter unit connected to the same SCSI controller card. If more than one formatter is used on a single SCSI controller, then the "subunit address" now becomes the unit address of each additional formatter that is connected,(0-3).

In the example above, the drive that would be addressed if this order was used would be:-

drive unit 0 on formatter 3 connected to the controller in VME 1 slot 2 on CCUxx.

6.26.4 Exabyte Tape Drives.

It may sometimes be hard to identify the difference between Single-ended, and Differential equipped drives, here are three ways that may help.

* Locate the white label on the top of the drive, this label carries the description of the various boards and code inside the drive. Down the list locate either the word "DIF" for differential, or "SIF" for single-ended, interface installed.

* View the back-end of the drive where the scsi cable plugs in to the interface. If there are only two or three positions for sip terminator resistor packs, then the drive has a single-ended interface installed. If there are five positions for sip terminator resistor packs, then the drive has a differential interface installed.

* If the above two methods do not prove to be of help, try viewing the back side, non-component side of the interface board, to see if the word "SIF" is printed on it, for single-ended.

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6.26.5 SPP1000/1200 "Timeout waiting on node communication"

```
+++>  1500
<Tue May 23 14:28:11 1995>  info:0x446d0005
/spp/bin/pulse_server:3.0.0.0:../pulse_server.c:228
Timeout waiting on node communication
****
```

/spp/bin/pulse_server is part of CXTS.

This message indicates the SPP-UX portion of the CXTS software is not setup and running or the SPP has crashed, hung or lost it's network.

You can rid yourself of these menacing messages by doing 1 of the following:

1. Setup CXTS on the teststation and SPP using the CXTS Version 1.6 Relase Notice. Doc. # 081-025630-006

2. Comment out the pulse_server entry in /etc/inittab on the teststation. init 4.

6.26.6 Convex Press I/O Web Announcement.

The "Convex Press I/O Web" (http://info.convex.com/io_doc/) provides online access to Convex I/O documentation from the Technical Assistance Center's "Convex Information Server" (http://info.convex.com/). The I/O Web home page is linked to "I/O Documentation" under "Convex Press/Documentation" on the server's "Information by Organization" page (http://info.convex.com/organizations.html).

The Elite 9 and QSC Service Guides are available now with others available soon.

The Elite 9 Service Guide pages have been updated and the QSC Service Guide will soon follow suit.

Comments and questions about the Convex Press I/O Web pages can be sent to "iomaster@convex.com".

6.26.7 QSC Released Product.

The QSC (Quad SCSI Channel) is now a released product. All associated software products have been released, as well.

These newly releaed software products are as follow:

1) Driver V1.0
2) 11.0 Miniroot tape
3) pLSI Database V1.3
4) Scsiutil V1.2

A new disk downloadable firmwave, V3.0, will be released soon. This will be supported by the Scsiutil release.

These products, combined, introduce dozens of bug fixes, improve performance and support root and swap, on scsi disks.

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6.26.8 C-Series Scsiutil Supports Disk Firmware Download.

With the release of V1.2 Scsiutil, it will be possible to download, directly, new disk firmware. In fact a new firmware, V3.0 will soon be released for the elite-9 drives. This new firmware will have several Seagate bug fixes, allowing the drives to be more robust.

The procedure for down loading new firmware is as follows:

1) Take system to SPU, as the firmware load is not supported, at the OS level.

2) Execute scsiutil.

3) from the scsiutil prompt, su 1>, open the disk, for this operation. For example, su 1> open sd0 sd1 sd2 sd3. This will allow the following instructions to execute on all selected drives. If the drives are not opened on the same command line, but one at a time, with separate open commands, it will be necessary to execute a "sel -o" to select the drives as follow:

4) Down load the firmware. For example: su 2> down E9FW1003.LOD. If the firmware file is not in the working directory, the full path will have to be specified.

5) Verify the download by, su 3> scr inq. This results in drive related status and info, with the last line indicating the revision level, in this case, 003.

6) The drives must then be closed. If the drives were selected by the open command, as in 1), then a close -o will be used. If the example below is used, just a close, is necessary.

NOTE If the drives are not opened on the same command line, but one at a time, with separate open commands, it will be necessary to execute a "sel -o" to select the drives as follow:

```
su 4> open sd0
su 5> open sd1
su 6> sel -o  <This selects sd0 and sd1>
```

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Contents of this issue:

1. KNOWN QSC DIAGNOSTIC FAILURES

6.27.1 KNOWN QSC DIAGNOSTIC FAILURES

It is possible to experience intermittent failures, with qsc4000, in subtest 2700 and 1410.

The failures will appear as follow:

```
Subtest   1    0:02:54   passed  Verify 1032 pLSI programs
Subtest   2    0:00:58   passed  Verify 2032 pLSI programs
Subtest 1000    0:00:00           Reset of QSC, EEPROM checksum & versi
Subtest 1100    0:00:20   passed  Data RAM bit functionality
Subtest 1110    0:00:00   passed  Data RAM column functionality
Subtest 1120    0:00:00   passed  Data RAM uniqueness
Subtest 1130    0:00:00   passed  Data RAM parity
Subtest 1200    0:00:23   passed  Instruction RAM bit functionality
Subtest 1210    0:00:00   passed  Instruction RAM column functionality
Subtest 1220    0:00:01   passed  Instruction RAM uniqueness
Subtest 1230    0:00:00   passed  Instruction RAM parity
Subtest 1300    0:00:08   passed  PMAP RAM bit functionality
Subtest 1310    0:00:00   passed  PMAP RAM column functionality
Subtest 1320    0:00:00   passed  PMAP RAM uniqueness
Subtest 1400    0:00:00   passed  PBUS header generation
Subtest 1410    0:00:00   failed  PBUS access

*****  Wed Apr  5 12:30:05 1995  *****
Test:  qsc4000.t  1.12   Class: 1  Subtest: 1410 1.18 Count: 1  Error: 0
Failed:  PBUS access
        ---------------------- Trace point: 1410.1 ----------------------
Error 0xe: Byte strobe test
32 bit access. Address 0x00400250 Expected 0x00010203 Actual 0x10000000

Test 'qsc4000.t' failed


Test:   qsc4000.t 1.12  Class: 2 Subtest: 2700 1.18 Count: 1 Error: 0
Failed: Microsecond counter and Line Clock Interrupt
    ----------------------Trace point: 2700.1 ----------------------
Error 0x13: Line clock interrupt test
51 line clock interrupts occurred in one second
Minimum time between interrupts was 19876 uS
Maximum time between interrupts was 20106 uS

Splits array:
0x27c696 0x2814a6 0x286286 0x28b0ae 0x28fea8 0x294d0c 0x299adf 0x29e934
.....
```

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Contents of this issue:

1. ACL2640 Automated Tape Library (DLT)
2. KNOWN Shortcomings with V1.0 QSC
3. SPP1200 Power Configuration
4. C4600 Errintd Hangs Debugging
5. SPP1200 check_for_apa_bugs can damage a SIOP2
6. SPP1000/1200 Diags and CST Version 3.2
7. New firmware available for Elite-9 Disks
8. C4600 Errintd Problem Solution
9. QSC Bulkhead Warning

6.30.1 ACL2640 Automated Tape Library (DLT)

Changes to the tape drivers since 11.0.3 have now made it a requirement that the SCSI addresses for the MUC and DLT drives in the ACL2640 robot follow the following form.

In the past the ACL robot was shipped to the customer with SCSI addresses of 2 for the MUC, and 3,4, and 5 for the three DLT drives. It is now a requirement that SCSI addresses can only be in the range of 0,1,2, and 3.

It has therefore been decided that future ACL2640 robots will be shipped from Dallas with the MUC addressed as unit 3, and drives addressed as units 0,1, and 2.

It should also be noted that the correct ioconfig entries for each device are as follows:-

```
Wiop 1
      Vme 0
        stlr MTC-200 csr 0xEA00 int 7
          unit 3 subunit 0 type SPT-001    (MUC robotic controller)
          unit 0 subunit 0 type MTD-220    (DLT drive that is capable of
          unit 1 subunit 0 type MTD-220       reading and writing
          unit 2 subunit 0 type MTD-220          compression tapes)
```

Many drive/MUC configurations are possible, this is just one example.

6.30.2 KNOWN Shortcomings with V1.0 QSC

There are two known problems, with the v1.0, released, QSC driver.

1) Redundant stripes are not supported, with this QSC driver version. This will be corrected in the v1.1 rlease, due in September.

2) A problem exists with mini-root, in that a raw installation cannot be accomplished, if unit 0 does not exist. This is very minor and should cause no problems, as long as this fact is understood.

6.30.3 SPP1200 Power Configuration

Although the SPP1200 system is configured as a 30amp system, for cost savings, it will be shipped as a 60amp system.

This should be understood, when any 1200 related site prep is accomplished.

6.30.4 C4600 Errintd Hangs Debugging

If an errintd hang should occur after loading the newest errintd process, it will be necessary to link the errintd process to the debugger and monitor this process until another hang occurs. This will be accomplished in a different window.

To accomplish this and provide useful information, it will be necessary to perform the following procedure:

Step 1. On a spu as diaguser type "errintd".

EXAMPLE:

```
spump> errintd

+++>
<Fri Jun  9 15:40:15 1995>   errintd(2484):../errintd.c:1066
SW Error (DiagER542): Errintd Already Running

Errintd Already Running, pid:      265
****
* * * * * Last command returned status 95 * * * * *
```

Step 2. type "gdb errintd xxxx" where xxxx is the process id.

EXAMPLE:

```
spump> gdb errintd 265
GDB is free software and you are welcome to distribute copies of it
under certain conditions; type "show copying" to see the conditions.
There is absolutely no warranty for GDB; type "show warranty" for details.
GDB 4.4, Copyright 1991 Free Software Foundation, Inc...


/users/diaguser/265: No such file or directory.
Attaching program: /diag/bin/errintd pid 265
Reading symbols from /usr/lib/libc.so.1.7...done.
Reading symbols from /usr/lib/libdl.so.1.0...done.
0xf77538d0 in select ()

(gdb)
```

6.30.4 C4600 Errintd Hangs Debugging(continued)

Step 3. Errintd is now suspended - start it up by "c"

EXAMPLE:

```
(gdb)c
Continuing.
```

Step 4. Open a second window on the spu
Step 5. Wait until a failure occurs.

Step 6. After a failure "kill xxxx" where xxxx is the errintd PID. This should produce a (gdb) prompt. At the prompt type "where". At the next prompt type "p State". Log the data.

EXAMPLE:

```
(gdb) where
#0  0xf77538d0 in select ()
#1  0x2418 in rpc_select () at ../errintd.c:194
#2  0x22d4 in main (argc=1, argv=0xf7fffa7c) at ../errintd.c:134

(gdb) p State
$1 = 2
```

Step 7. Get the message status in the other window with "ipcs"

EXAMPLE:

```
spump> ipcs
       IPC status from spump as of Fri Jun  9 16:01:36 1995
       T     ID     KEY        MODE       OWNER    GROUP
       Message Queues:
       q      0 0x000000a5 -Rrw-rw-rw-     root     wheel
       q      1 0x00000183 -Rrw-rw-rw-     root     wheel
       q      2 0x420002e1 -Rrw-rw-rw- diaguser diaguser
       Shared Memory:
       m      0 0x4168e01b --rw-rw-rw-     root     wheel
       Semaphores:
       s      0 0x51054201 --ra-ra-ra- diaguser diaguser
       s      1 0x4105d6aa --ra-ra-ra- convexos diaguser
```

**********NOTE**********

This should only be accomplished if errintd related hangs continue, after installing the newest available errintd, found in /common/tachwsup.

6.30.5 SPP1200 check_for_apa_bugs can damage a SIOP2

A bug has been found that can actually damage the SIOP2 in SPP1200's.
Please remove/delete /spp/scripts/apa/check_for_apa_bugs from all SPP1200's immediately.
This bug will be fixed in the next Diag release(greater than 3.2.)

6.30.6 SPP1000/1200 Diags and CST Version 3.2

SPP1000/1200 Diags and CST Version 3.2 has been released.
This version is mandatory for all SPP1200's. It is optional(at this time) for SPP1000's but because it contains some new debug scripts it is recommended that it be loaded on SPP1000's running SPP-UX 3.0 or higher.

You may retrieve 3.2 Diags/CST and the release notice via ftp.

```
-Convex WAN-

ftp lurch

username: ftp
password: your_email_address

cd /pub/Diags_3.2
get Diags_3.2.sd.gz
get rel_3_2.body.ps

*** Installation ***

Note: you must be root and all sd files are assumed to be in /tmp on
      the teststation.


1)  shutdown the SPP

        /etc/reboot -h

2)  gunzip /tmp/Diags_3.2.sd.gz

3)  Bring teststation to single user mode

       /etc/shutdown

4)  install the Diags

        cd /
        /etc/installsw -s /tmp/Diags_3.2.sd

        Hit <RETURN> at the prompt

5)  Reboot the teststation

        /etc/reboot
```

6.30.6 SPP1000/1200 Diags and CST Version 3.2(continued)

Allow the teststation to reboot and establish contact with each node connected. Allow the "database regeneration" to complete for each node.

6) use "node_info" to verify each node is talking to the teststation.

7) For each node do:

```
load_mufw "node_id"
load_pl "node_id"
```

8) do_reset 1

Allow the teststation to reboot and establish contact with each node connected. Allow the "database regeneration" to complete for each node.

9) Use cmu to configure each nodes MU.

```
cmu
cmu> pull
cmu> up
cmu> auto
```

If any "not as expected" messages appear, use the "put" command to correct these inconsistencies. Repeat the "auto" and "put" command until "auto" completes without further "not as expected" messages. Time-out disabled messages are ok.

```
cmu> down
cmu> push
cmu> quit
```

10) do_reset

6.30.7 New firmware available for Elite-9 Disks

Version 3.0 disk firmware is now available, from Seagate, for the Elite-9 SCSI disks, used with the QSC. The product name is "FW Elite-9 download 3" version 1.0. This product can be ordered now and will include the firmware E9FW1003.LOD.

For those that do not wish to wait for a tape and all of the prereq's are met, this firmware is available in /common/tachwsup.

The prerequisites, for this loading this firmware, is as follows:

1) v1.0 QSC driver
2) v1.2 Scsiutil
3) v1.3 pLSI database

6.30.7 New firmware available for Elite-9 Disks(continued)

The procedure for down loading new firmware is as follows:

1) Take system to SPU, as the firmware load is not supported, at the OS level.

2) Execute scsiutil.

3) from the scsiutil prompt, su 1>, open the disk, for this operation. For example, su 1> open sd0 sd1 sd2 sd3. This will allow the following instructions to execute on all selected drives. If the drives are not opened on the same command line, but one at a time, with separate open commands, it will be necessary to execute a "sel -o" to select the drives as follow:

4) Down load the firmware. For example: su 1> down E9FW1003.LOD. If the firmware file is not in the working directory, the full path will have to be specified.

5) Verify the download by, su 3> scr inq. This results in drive related status and info, with the last line indicating the revision level, in this case, 003.

6) The drives must then be closed. If the drives were selected by the open command, as in 1), then a close -o will be used. If the example below is used, just a close, is necessary.

NOTE If the drives are not opened on the same command line, but one at a time, with separate open commands, it will be necessary to execute a "sel -o" to select the drives as follow:

```
su 4> open sd0
su 5> open sd1
su 6> sel -o  <This selects sd0 and sd1>
```

6.30.8 C4600 Errintd Problem Solution

As reported in previous bulletins, it is possible for errintd to hang, while processing a soft, or assisted error, due to corruption of the configuration mask.

It is now believed that this problem can be resolved by allowing time for the mask to stabilize, before accessing it. A new errintd is available which does this by waiting for one second before accesses to this register are attempted.

If problems should arise, with this new errintd, it is also configured for the debugger. Setting up for debug will be detailed in a later tech bulletin.

For now, this errintd is available on-line, in the /common/tachwsup directory. It is recommended that this file be retrieved and installed, asap, as this may relieve many system hangs.

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6.30.8 C4600 Errintd Problem Solution(continued)

It is possible to install this utility with the system up. To do this, simply rename the current /diag/bin/errintd process to another file and place the new one in it's place. Then kill the existing process and allow the new one to started, in it's place.

A sum of this file is, 20736 1168.

6.30.9 QSC Bulkhead Warning

A problem exists with all installed QSC bulkheads. This problem is potentially serious, if for any reason it is necessary to separate the EMI cover, from the circuit board.

The problem is that as these two components are pressed together, it is possible for the EMI gasket, between the parts, to spread and short pins on the connector. As power is applied through this connector, it is possible to damage the bulkhead and the CCU/Bulkhead cable to connector P5.

This problem is resolved on all future bulkheads, by using a different gasket material, which will not expand.

In the meantime, if for any reason it is necessary to disassemble the bulkhead assembly, it is highly recommended that mylar, or electrical tape be used to cover the connectors, on this component. This will eliminate the possibility of a short.

The long term solution will be to replace all existing bulkheads with the newer ones.

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Contents of this issue:

1. SPP1000/1200 Revised Gatearray Torque Spec
2. FSC codes for QSC on C-Series
3. C4 APR Deficiencies
4. Clearing C3800/C4600 soft_log

6.31.1 SPP1000/1200 Revised Gatearray Torque Spec

SPP1000/1200 Revised Gatearray Torque Spec

Since some SPP systems have experienced gatearrays coming loose during shipping and operation, the gatearray torque specification has been revised to 7 in/lbs. Please torque all SPP1000/1200 gatearrays to 7 in/lbs during your next site visit for PM or corrective maintenance.

6.31.2 FSC codes for QSC on C-Series

This is a list of the 9 current Fault Symptom Codes, which can be reported by the QSC driver.

0x0006 (No such device)
Reported by procdev.

0x1001 (LUN not found)
The QSC supports 64 LUNs per device and a maximum of 400 LUNs for all devices total. This error indicates that an attempt was made to access more that 400 LUNs for this QSC board.

0x1002 (Unit not found)
Select/reselect error. Check SCSI ID. Indicates that access is requested to a non-existent device. Wrong SCSI ID set.

0x1017 (Unknown MBS message)
Unknown command.

0x1028 (Memory allocation)
Not enough memory to cover outstanding command limit. Could not allocate an io_request structure. There should be one allocated for each possible outstanding io request at system initialization.

0x1029 (Channel memory allocation failed)
Memory resources were not available to complete this request.

A configuration problem. Check the statistics on the QSC using adbccu to determine which type of memory resource allocation failed.

0x1111 (Channel error)
Similar to 2222, but on any SCSI channel.

6.31.2 FSC codes for QSC on C-Series (continued)

0x2222 (MPU channel error on port 4)
Channel buffer asserted CH_PB_BUFERR during a transaction.

0x3333 (Phase mismatch)
NCR SCRIPTS attempted an operation that did not match the SCSI bus phase of the target.

6.31.3 C4 APR Deficiencies

As reported in previous tech bulletins, the cpu_monitor daemon is not included in 11.1 OS and must be loaded by means of the existing tac patch.

In addition, the cpualloc.test utility does not exist on the workstation. For this reason it is not possible for cpu_monitor to initiate sst tests, on a failed head. Because of this it is necessary to set SST_ENABLE = 0, in /etc/cpu_monitor.config file.

Besides these two restrictions, it should be understood that it is not possible for cpu_monitor to return a failed head to the OS automatically. The APR function will take the head off-line, but the processor must be returned to the configuration manually, by using cpuconf.

This should be an extremely minor disadvantage, as the soft SPR error handling, assisted errors and the reliability of the system makes the automatic recovery almost redundant.

This shortcomings should be addressed in the next diagnostic release.

6.31.4 Clearing C3800/C4600 soft_log

Is is well known, the soft_clean utility is used to clear the soft_log on C3800's and C4600's. But it should be understood that the soft_clean utility is nothing more than a script and is used to remove specific CDB entries. These CDB entries store the actual soft error info, for memory, I/O and processors.

So, because soft_clean is only a script, it can be created very easily. This can be important, as it is possible to have this script removed, particularly, as it is missing from the 4.1 diagnostic release, so virgin installs will remove it.

The script really existed to clear a limited number of soft error entries, such as memory and processor and leave other alone, such as IA soft errors.

This script should be placed in /diag/hw, on both platforms.

6.31.4 Clearing C3800/C4600 soft_log (continued)

In cases where the soft error entries, in the CDB are all used, it is possible to clear all entries by dump_soft_log -i.

If it is desired to remove individual entries, the soft_clean script can be recreated very easily, by understanding the individual entries. An example of a 3800 script is shown below.

```
#!/diag/bin/dsh

# These are the individual emmory soft error entries. Each 0 represents
  individual memory errors. These entrries range from 0-59.

 cdb_update soft_error_0 0 0 0 0 0 0 0 0
 cdb_update soft_error_1 0 0 0 0 0 0 0 0
 cdb_update soft_error_2 0 0 0 0 0 0 0 0
 cdb_update soft_error_3 0 0 0 0 0 0 0 0
 cdb_update soft_error_4 0 0 0 0 0 0 0 0

# Below are IA_soft error entries and range from 0-48. Each 0 represents
# a different NIA slot 0-8, which can exist in the system. Most will
# only have to worry about IA8, but all other preceeding 0's will have
# to be used.

 cdb_update ia_soft_error_0 0 0 0 0 0 0 0 0
 cdb_update ia_soft_error_1 0 0 0 0 0 0 0 0
 cdb_update ia_soft_error_2 0 0 0 0 0 0 0 0
 cdb_update ia_soft_error_3 0 0 0 0 0 0 0 0

# Below lines are to remove sp_soft_errors, 0-7. These errors can only
# be logged with XCL2 and 8247 NSP's installed.

 cdb_update sp_soft_error_0 0 0 0 0
 cdb_update sp_soft_error_1 0 0 0 0

# Below are miscellaneous error counts and entries which should be
  removed.

 cdb_update errors_not_logged 0
 cdb_update total_failures 0
 cdb_update failed_devices 0
 cdb_update first_logged_failure 0 0 0 0 0 0 0 0
 cdb_update last_logged_failure 0 0 0 0 0 0 0 0

 exit 0
```

Although the soft_clean should not be removed, on the C4, an example of the soft_clean script is shown below. With the prvious explanation, entries should be obvious. Consult the CDB for all entries possible.

6.31.4 Clearing C3800/C4600 soft_log (continued)

```
#!/diag/bin/dsh

cdb_update smbc_soft_error_0 0 0 0 0 0
cdb_update smbc_soft_error_1 0 0 0 0 0
cdb_update smbc_soft_error_2 0 0 0 0 0
cdb_update smbc_soft_error_3 0 0 0 0 0
cdb_update spr_soft_error_0 0 0 0
cdb_update spr_soft_error_1 0 0 0
cdb_update spr_soft_error_2 0 0 0
cdb_update spr_soft_error_3 0 0 0
cdb_update sdcc_errors_not_logged 0
cdb_update smbc_softerr_not_logged 0
cdb_update total_sdcc_failures 0
cdb_update failed_sdcc_devices 0
cdb_update first_logged_failure 0 0 0 0 0 0 0 0 0 0
cdb_update last_logged_failure 0 0 0 0 0 0 0 0 0 0
cdb_update sdcc_log_entry_0 0 0 0 0 0 0 0 0 0 0
cdb_update sdcc_log_entry_1 0 0 0 0 0 0 0 0 0 0
cdb_update sdcc_log_entry_2 0 0 0 0 0 0 0 0 0 0
cdb_update sdcc_log_entry_3 0 0 0 0 0 0 0 0 0 0
cdb_update sdcc_log_entry_4 0 0 0 0 0 0 0 0 0 0
cdb_update sdcc_log_entry_5 0 0 0 0 0 0 0 0 0 0
cdb_update sdcc_log_entry_6 0 0 0 0 0 0 0 0 0 0
cdb_update sdcc_log_entry_7 0 0 0 0 0 0 0 0 0 0

exit 0
```

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Contents of this issue:

1. ACL-2640/DLT Switch Settings
2. FMI0110 and FMI0111

6.32.1 ACL-2640/DLT Switch Settings

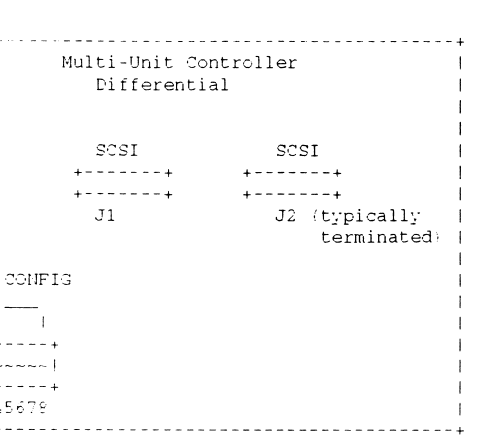

Figure 1: MUC Front View

Switch	Definition
1,2, and 3	SCSI ID (See Table 2)
4,5, and 6	Reserved
7	Host Selection (Down=SCSI Host, UP = Serial Host)
8	Reserved

Table 1: MUC Dip Switch Settings

LS Bit SW 1	SW 2	MS Bit SW 3	SCSI ID
DOWN	DOWN	DOWN	0
UP	DOWN	DOWN	1
DOWN	UP	DOWN	2
UP	UP	DOWN	3

Table 2: MUC SCSI ID (Switches 1, 2, and 3)

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6.32.1 ACL-2640/DLT Switch Settings(continued)

Note: Recycling the MUC power is required after re-setting the SCSI IDs.

Special Note: These addresses are THE ONLY ONES supported for this product.

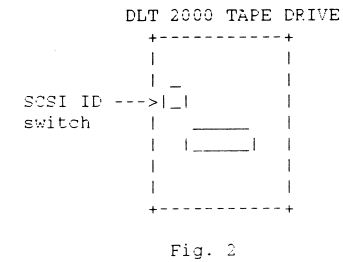

Fig. 2

Fig. 2A
SCSI ID SWITCH
* denotes push button

6.32.2 FMI0110 and FMI0111.

FMI0110 and FMI0111 have been released. Copies of these FMI's will be sent to each field office in the next week.

FMI0110

Title: SPP1000 XBAR2 Upgrade

Purpose of Change:
Prevent a CCMC buffer overrun when a SIOP1' (410-004376-200) or a SIOP2 (410-005376-200) is installed in a SPP1000 node.

Priority:
Mandatory for SPP1000 nodes being upgraded to a SIOP1' or SIOP2.

FMI0111

Title: SPP1000 SIOP Upgrade

Purpose of Change:
To prevent a potential hang when more than one SCSI controller is installed on a unit, i.e. one half of the SIOP1.

Priority:

Mandatory for SPP1000 systems with 3 SCSI controllers on a SIOP1(410-002376-200).

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Contents of this issue:

1. SPPRING Class 6 and 7 False Failure
2. CST Version 3.3 bugs
3. SPP1000/1200 Upgrade Configuration Requirements/Restrictions
4. DLT(Digital Linear Tape) Drive Problem

6.34.1 SPPRING Class 6 and 7 False Failure

A bug has been found that may cause sppring class 6 and class 7 failures. There is a timing problem causing a diagnostic access to have corrupted data.
^^^^^^^^^^

In general, this hardware bug will affect ALL subtests in class 6 and 7. The symptom is the test will complain about wrong tag info. If you see this, you might want to re-run the test to verify. If it runs for 5 loops, you can assume the hardware is OK.

6.34.2 CST Version 3.3 bugs

When running CST 3.3 you may encounter the following error messages. These msgs will appear in the xterm window you started cst in and the event_log.
These messages DO NOT effect CST and may be ignored.

Message 1.

```
pce_util:   3.3 (Wed Aug  2 16:33:04 1995)
scan_lock failed on at least one node - returned -1, errno = 0x 495 (1173)
errno is 0x495 (1173)
this could be the MU error code MU_STATUS_SCAN_IN_USE
+++>  413
<Fri Aug 25 10:56:10 1995>  warning:0x65660425
pce_util:3.3.0.0:../scan_q_node.c:107
actual event logged from ../scan.c:203 [scan_error ()]
noted module/line numbers are for routine scan_q_node
received a return code of 0xffffffff (-1) - errno is 0x494 (1172)
errno is 0x494 (1172)
this could be the MU error code MU_STATUS_SCAN_NOT_OWNER
in call to scn_write for putting 0 rings in IDLE
node: 3
```

Message 2.

```
+++>  161
<Wed Aug 23 23:21:10 1995>  warning:0x67600510
<MU FW>:3.3.1.0:sci_error.c:473
node: 0x1 (1)
Error received from SCI ring 0
ERR_STAT: 0x00002000
****
```

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6.34.4 SPP1000/1200 Upgrade Configuration Requirements/Restrictions

SPP1000 Single Node to 4 or Less SPP1000 Nodes

When upgrading from a SPP1000 Single Node to 4 or Less SPP1000 nodes, the following parts will need to be the correct revision and may need to be upgraded or installed when installing additional Nodes.
CSB4, SCAM cards, CPA(agent ASIC), CCMC2(coherency and memory control ASIC), SCI(coherent interconnect ASIC), MU/MU2(utilities board) and PB2(power board.) See table 1 for the required revisions of these parts.

SPP1000 Less Than 4 Nodes to Greater Than 4 SPP1000 Nodes

When upgrading from a SPP1000 with Less Than 4 Nodes to Greater Than 4 SPP1000 Nodes, the following parts will need to be the correct revision and may need to be upgraded when installing additional Nodes. CSB4, CPA(agent ASIC), CCMC2 (coherency and memory control ASIC), SCI(coherent interconnect ASIC), MU/MU2(utilities board) and PB2(power board.)
See table 2 for the required revisions of these parts.

SPP1000 Node to SPP1200 Node

When upgrading from a SPP1000 Node to a SPP1200, the MTV's(memory), MU/MU2, and SBUS controllers will be moved from the SPP1000 Node to the SPP1200 Node. The MU/MU2 will need to be the correct revision and may need to be upgraded.
See table 3 for the required revisions of these parts.

SPP1000/SPP1200 Mixed Node Systems

Not Supported

SPP1000 SIOP1 to SIOP1' or SIOP2

When upgrading a SPP1000 Node from a SIOP1 to a SIOP1' or SIOP2, the CXbar in the XBS(Z102K8) location will have to be upgraded to a CXbar2.
See table 4.

SPP1000 SIOP1 Less than 3 SBUS SCSI's to 3 or More SBUS SCSI's

When upgrading a SPP1000 Node with a SIOP1 and less than 3 SBUS SCSI's to 3 or More SBUS SCSI's, the SIOP1 will have to be upgraded to a SIOP1' or a SIOP2. See table 5.

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SPP1000 Single Node to 4 SPP1000 Nodes or Less		
CSB4	410-001396-200	Rev D. or Higher
SCAM Cards	410-002473-200	
CPA REV C	550-000096-210	
CCMC2 REV B	550-000095-210	
SCI REV B or SCI REV C	550-000093-210 550-000093-220	
MU or MU2	410-003375-200 410-002375-200	Rev B. or Higher Rev A. or Higher
PB2	410-002380-200	

Table 1.

SPP1000 Less Than 4 Nodes to Greater Than 4 SPP1000 Nodes		
CSB4	410-001396-200	Rev D. or Higher
CPA REV C	550-000096-210	
CCMC2 REV B	550-000095-210	
SCI REV C	550-000093-220	
MU or MU2	410-003375-200 410-002375-200	Rev B. or Higher Rev A. or Higher
PB2	410-002380-200	

Table 2.

SPP1000 Node to SPP1200		
MU or MU2	410-003375-200 410-002375-200	Rev C. or Higher Rev B. or Higher

Table 3.

6.24.1 SPP1000/1200 Upgrade Configuration Requirements/Restrictions(contd)

SPP1000 SIOP1 to SIOP1' or SIOP2		
CXBAR2	550-001008-210	Rev A. in XBS(Z102K8)

Table 4.

SPP1000 SIOP1 Less than 3 SBUS SCSI's to 3 or More SBUS SCSI's		
CXBAR2	550-001008-210	Rev A. in XBS(Z102K8)
SIOP1' or SIOP2	410-004376-200 410-006376-200 410-005376-200 410-007376-200	

Table 5.

6.34.4 DLT(Digital Linear Tape) Drive Problem

A problem has been identified when a customer uses a DLT drive on a C2 series system.

The s/w driver will currently only recognize a drive during the probe-and-attach phase of a C2 boot process, if the drive contains a tape cassette.

The problem has been corrected and a fix should be available soon

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Contents of this issue:
1. SPP1000/1200 Disk Online Test Utility (diskf)
2. SPP1200 ccmd Error Message
3. SPP1200 mu_fw 3.3 APA Timeout after pce_util -p off

6.37.1 SPP1000/1200 Disk Online Test Utility (diskf)

"diskf" is very basic on-line disk test utility available for SPP-UX on SPP1000/1200 systems. "diskf" is not a "released" product, but should give you some test capabilities not currently available. This utility will be helpful when wanting to exercise the disk subsystem after any upgrade or when trying to reproduce a disk failure.
diskf should be loaded on each system, in a "Convex maintenance account".

DESCRIPTION:
diskf performs and times write and read operations to disk. Exactly how this happens is based on data provided by the user, either prompted by diskf or via some command file.

diskf may be retrieved via the Convex Wan.

```
ftp lurch

username: ftp
password: your_email_address

cd /pub/utilities
get diskf
```

diskf -u will show the usage.
diskf -h will print the help file.

Please read the complete help file before executing diskf.

6.37.2 SPP1200 ccmd Error Message

Diags/mufw 3.3 has a bug that will produce the following message when ccmd is building the configuration database.

```
+++>  267
<Wed Sep  6 13:08:48 1995>  warning:0x656a0443
/spp/bin/ccmd:3.3.0.0:../check_current_config.c:1046
DB line does not start with 'PART ' when looking for JTAG ID 0x1993e0d1
ring: 1    DB_ring file: /spp/data/DB_ring.asb
processed 0 parts before failing
****
```

This meeasge can be safely ignored.
This bug will be corrected in the next Diags/mufw release.

6.37.3 SPP1200 mu_fw 3.3 APA Timeout after pce_util -p off

mu_fw version 3.3 has some code that monitors for hung APA's.
When the node is powered off via "pce_util -p off" you will many of the following messages in the event_log.

```
+++>  171
<Wed Sep 13 13:38:27 1995>  warning:0x67602001
<MU FW>:3.3.1.0:apa_ping.c:97
node: 0x0 (0)
CPU 1 APA timeout register write failed with status 0x3a6 (934)
****
```

At least 1 of these messages will be placed in the event_log for each cpu in the system. This timeout occurs because the mu_fw can not write to a chip that has been powered off. This will be corrected in the next release of the Diags/mu_fw. Until then, this message can be safely ignored if it is the result of powering off a node or system.

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Contents of this issue:

1. SPP Disk and Tape Configuration Limits
2. C4 io5000.t warning

6.38.1 SPP Disk and Tape Configuration Limits

Although the SCSI Fast and Wide Spec allows up to 16 devices(including the SCSI cntrl) to be attached, the SPP I/O system imposes additional limits. These limits are outlined below.

Convex only supports disk and tape devices available through the marketing "Exemplar Product Catalog" or via a quote from "CXServices".

Single Ended Fast and Wide SCSI

There is a limit of 5 disks and 1 DAT attached to a SE F/W cntrl. These devices must be mounted in a Convex SPP1000/CD IO CHASSIS. No other Single Ended Fast and Wide SCSI configurations are supported.

Differential Fast and Wide SCSI with a Convex SPP1000/XA IO CHASSIS

Because the physical unit addresses are hardwired into the SPP1000/XA IO CHASSIS, there is a physical limit of 10 disks and 1 DAT connected to each Differential Fast and Wide SCSI cntrl.

Differential Fast and Wide SCSI with External Devices.

Differential Fast and Wide SCSI on a SIOP1 will only support up to 13 logical devices(including the SCSI cntrl). This is due to a hardware/software limitation.

Differential Fast and Wide SCSI on a SIOP2 will support up to 16 logical devices(including the SCSI cntrl).

The maximum total cable length for Differential Fast and Wide SCSI is 25 meters. This includes any cable length internal to the peripheral devices or cabinets.

6.38.2 C4 io5000.t warning

It is possible for the io5000.t diagnostic to hang the SPU, in class 4 of the test, if run in any unclear state. This means that an initall should be executed prior to all iterations of the diagnostic. This will increase risk of looping on any subtest in class 4, as well.

This problem is intermittent and is most likey to occur during a very involved troubleshooting scenario.

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Contents of this issue:

1. SPP1200 ASB PLL Clock Mode Configuration
2. SPP1200 MU Firmware 7.0.3(Diags 7.0)

6.39.1 SPP1200 ASB PLL Clock Mode Configuration

The Motorola PLLs, on the ASB board, support two modes. One mode (3:2) allows running the system with 100MHZ 'P' Modules and the other mode (4:3) allows the system to run with 120MHZ 'P' Modules.

The ASB was designed to use zero ohm SMT resistors to strap the mode for the PLLs. Due to the possibility of ASBs needing to be upreved to 120MHZ in the field the zero ohm resistors were removed on the mode bits that would change. Instead of resistors, 30 gauge wires are used in hopes these will be easier to remove and install in the field.

There are currently three different ASB types in the field:

- 410-0001455-200 wire rev A.
- 410-0002455-200 wire rev C. Note: These are "wire revs" not "assy revs"
- 410-0002455-200 wire rev D.

In the following tables 1 = connect and 0 = open

410-0001455-200 wire rev A PLL Clock Mode Configurator

Reference Designator	3:2 Mode (100MHZ) Install	4:3 Mode (120MHZ) Install
Z052K0	1	0
Z052K1	0	1
U029L7	1	0
U029L6	1	1
U029L5	0	1
U029L4	1	0
U029L3	0	1
U029L2	0	0
U029L1	1	1
U029L0	0	1

NOTE: All wires are easily accessed on the U-side of the board other than Z052K0 and Z052K1 which are on the opposite side of the board. These two also have another distinction in that they are not zero ohm resistors. So to accomplish a clock mode change in the field a cut has been made from one side of the resistors to separate it from the signal wire in the factory. The connection is made on these two by adding a wire from the appropriate side of the resistor to its signal via hole.

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6.39.1 SPP1200 ASB PLL Clock Mode Configuration(continued)

410-0002455-200 wire rev C PLL Clock Mode Configurator

Reference Designator	3:2 Mode (100MHZ) Install	4:3 Mode (120MHZ) Install
U029L9	0	1
U029L8	1	0
U029L7	1	0
U029L6	1	1
U029L5	0	1
U029L4	1	0
U029L3	0	1
U029L2	0	0
U029L1	1	1
U029L0	0	1

NOTE: All wires are easily accessed on the U-side of the board.

410-0002455-200 wire rev D PLL Clock Mode Configurator

Reference Designator	3:2 Mode (100MHZ) Install	4:3 Mode (120MHZ) Install
U026L7	0	1
U026L6	0	0
U026L5	1	0
U026L4	0	1
U026L3	1	0

U026L2	1	1
U026L1	0	0
U026L0	0	0

6.39.1 SPP1200 ASB PLL Clock Mode Configuration(continued)

410-002455-200 wire rev D PLL Clock Mode Configurator

Reference Designator	3:2 Mode (100MHZ) Install	4:3 Mode (120MHZ) Install
U029L9	0	1
U029L8	1	0
U029L7	1	0
U029L6	1	1
U029L5	0	1
U029L4	1	0
U029L3	0	1
U029L2	0	0
U029L1	1	1
U029L0	1	1

NOTE: All wires are easily accessed on the U-side of the board.

6.39.2 SPP1200 MU Firmware 7.0.3(Diags 7.0)

There is a bug in the SPP 7.0.3 mu firmware that will cause OBP traps after power up or a do_rest 1. The temporary work around is to execute do_reset 3 until OBP starts up and successfully synchronizes all nodes. It might take several do_reset 3's to be successful.

FIELD SUPPORT TECHNICAL BULLETIN

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Contents of this issue:

1. MTV Removal Warning for SPP1000/1200's
2. Elite9 Disk FRU Change
3. FM0111-A SPP1000 SIOP1 Upgrade Released
4. C4600 QPC Interface Cables

6.41.1 MTV Removal Warning for SPP1000/1200's

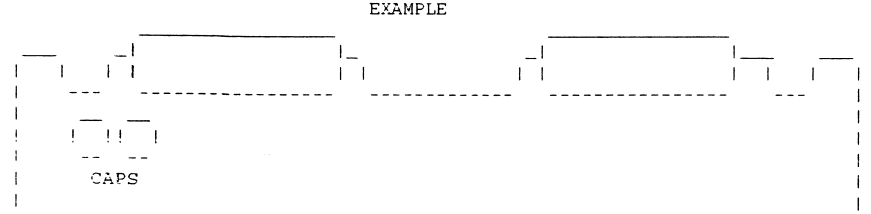
Capacitors exist on the solder side of the wire rev A MTV's, which are required for noise reduction. Without these caps, the MTV's will be susceptible to intermittent and random single and double bit ECC errors.

This is important to understand, because in the 0, or bottom position, it is very easy to knock these caps off, due to poor clearance on a single pem nut, on the right hand bottom side of the node.

This damage can be avoided by ensuring that upward pressure is maintained on the MTV during the entire removal process. This will allow the caps, on the connector side of the board, to easily clear this obstacle, when removed.

Because the damage can be so subtle and thus go unnoticed, it is recommended that all wire rev A MTV's be inspected and a replacement ordered, if one. or more of the caps are found missing.

EXAMPLE



SOLDER SIDE

NOTE Caps would be on opposite side, from this when installed in system, as MTV is installed component side up.

To verify rev A boards, the cop can be utilized. The wire rev is listed under the "wr" header.

Although the damage will only occur on MTV's in slice 0, it is recommended that all boards be checked, as memory boards may have been rotated within the system.

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6.41.2 Elite9 Disk FRU Change

Due to a connector configuration change, by Seagate, to this drive, it is necessary to change the front panel cable, used in the disk enclosure. As this cable is difficult to replace, the FRU is being changed,

The old FRU was 550-002290-297, which was the disk only. The new FRU, 550-002290-200, will include the enclosure.

The elite9 drive is a SCSI drive, currently used only with the QSC.

6.41.3 FM0111-A SPP1000 SIOP1 Upgrade Released

FM0111-A has been Released. Copies of this FMI will be sent to each field office within the next 2 weeks.

Differences between FM0111 and FM011-A are as follows:

Required Parts was changed to 410-004376-200 or 410-006376-200

Prereqs SPP-UX 3.1 and Diags 7.0 were added. This is to support the 410-006376-200.

6.41.4 C4600 QPC Interface Cables

To avoid intermittent, quadrant oriented, false power failures, during boot, it is recommended that the QPC-SPR and/or QPC-SMB interface cables be removed from positions where the board is not installed.

This means that if a SPR is installed in a quadrant and the memory board is not installed, then this cable should not be placed in the power foreplane test position, but removed altogether.

If this cable is left in the test position, it is possible to encounter a power related problem, indicating a failure with the installed component, in this quadrant. This will lead to unnecessary down time.

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Contents of this issue:

1. SPP Differential I/O Chassis

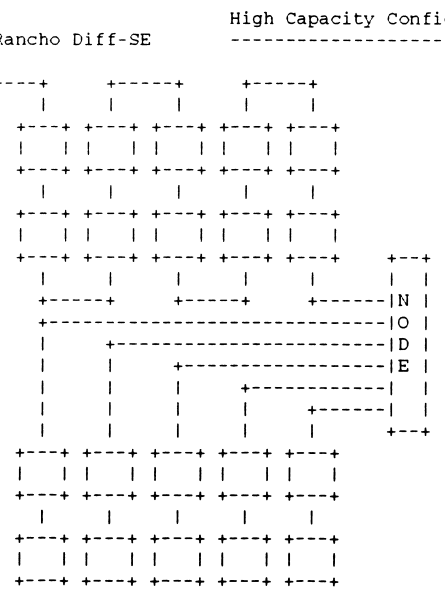
6.42.1 SPP Differential I/O Chassis

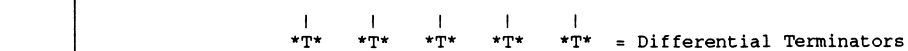
The differential I/O chassis will replace the current S.E. I/O chassis in production shipments in Q3, Q4 1995. The new chassis will reduce the complexity and allow for additional flexibility in customer configurations.

The differential I/O chassis appears similar to the existing I/O chassis. The I/O bulkhead has been changed to facilitate connection of the differential disk drives. All six "Ancot Diff. to Single" converter boards have been removed, and one new "Rancho Board, Differential to Single -Ended Converter" has been installed. This new converter provide the single-ened conversion for the DAT drive. A second "Rancho Board" can be installed if you require DATs on separate busses. This change has allowed for removal of the 5v Booster power brick, due to the reduced power load requirements.

A bright orange label with the designation "'DIFFERENTIAL', Convex p/n 021-000255-001", shall be applied to all drives and disk chassis to aid service and installation personnel in distinguishing the new differential chassis from the earlier single-ended chassis.

The differential I/O chassis may be configured to maximize performance an/or capacity. Although other configurations are possible. Block diagrams of two of the possible configurations are shown below.





High Performance Configuration

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6.42.1 SPP Differential I/O Chassis

The removal/installation procedures for the differential I/O chassis are the same as those for the existing single-ended chassis.

The differential I/O chassis FRU's are listed in the following table.

Description	Convex part number
Peripheral Assembly, I/O Chassis, Diff	550-000051-201
Converter, 48v/5v 200 w Sht Stud Driver	200-001047-209
Converter, 48v In 12v out 200w Boost	200-001047-211
Converter, 48v In 12v out 200w Drv	200-001047-212
Board Assembly, CIOPC	410-001442-200
Cable Assembly, SCSI, 14', HD68POS-SAME	602-680001-201
Assembly, Fan, I/O Chassis	500-000074-200
Rancho Board, Differential to Single Ended Converter	201-000004-201

For those of you with access to the Convex web pages, you can view this and additional I/O information using "http://info.convex.com/io_doc/".

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Volume: 6 Week: 44 Page: 1 of 3

Contents of this issue:

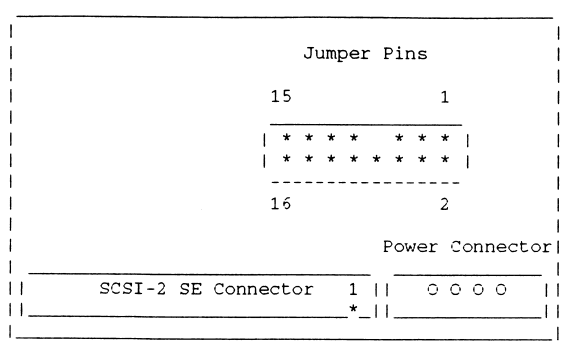
1. Dat Drive Replacement
2. Metrum RSP-2150 Drive Firmware
3. Important Metrum (now MountainGate) Field Issues!

6.44.1 Dat Drive Replacement

A new Conner Dat Drive is now available and is a direct replacement for the earlier Conner model 4326RP, Convex PN 207-000031-200.

The new Conner model is CTD8000R-S, Convex PN 207-000041-200.

Configuration Information is as follows:



Jumper Configuration:

Pins 15-16 = In (Termination Power on)
Pins 13-14 = Out (No Connection)
Pins 11-12 = In (Active Termination enabled)
Pins 9-10 = In (Data Compression disabled)
Pins 8-10 = Out (Power-On Self Test enabled)
Pins 5-6, 3-4, 1-2 = SCSI ID bits, according to Table 1.

TABLE 1

PIN 5	PIN 3	PIN 1	SCSI ID
6	4	2	
off	off	off	0
off	off	on	1
off	on	off	2
off	on	on	3
on	off	off	4
on	off	on	5
on	on	off	6
on	on	on	7

6.44.1 Dat Drive Replacement(continued)

Notes:

- Pin 7 is omitted
- The drive must be power cycled in order for the new jumper settings to take effect.
- If the dat drive will be replaced in a Sparc Station SPU then set the SCSI ID to 4 (5-6 in, 3-4 out, 1-2 out).
- Jumpers on pins 11-12 (Active termination enabled) is for SPP Diff I/O chassis. This jumper should be removed for Sparc Station SPU, SPP SE I/O chassis and C-series 4-drive cabinet. (If the dat drive is not at the end of a SCSI bus, pins 11-12 should NOT be jumpered.)

6.44.2 Metrum RSP-2150 Drive Firmware

In order for Convex to get some credit for upgrades to V5.2 of the Metrum firmware, we need to know if you HAVEN'T been upgraded. If we don't receive your input, we will assume that you have been upgraded to V5.2. If your customer drives need the upgrade, please place an order through your local logistics office, and copy kgipp on the mail. The part number to order is 207-000023-008.

This version of the Metrum firmware is backward compatible with all versions of the Unitree software, as well as being a requirement for Unitree version 2.0 sites.

6.44.3 Important Metrum (now MountainGate) Field Issues!

From Convex Engineering

Convex has been working with MountainGate on several issues to decrease field failures for the RSP2150 drives. We wanted to pass this along to the field.

This field bulletin discusses two specific changes to the product which affects the field. One issue is a change in the requirement for depot repair. The second issue is to update the field on media compatibility issues with the RSP2150 drives which have some changes that could help customers with T180 tapes. Lastly, there is some discussion on other changes coming in the near future which we need some field input.

Item 1: Changes in Depot Preventive Maintenance (3000 hr PM or 50,000 wraps)

MountainGate suggests that RSP2150 drives be returned for depot repair for drives reaching 3000 tape motion hours OR 50,000 WRAPS. The change here is

to return drives for 50,000 wraps. This data is accessible via the drive display panel. Now drives need to be returned for depot (MountainGate) repair if it reaches 50,000 wraps or 3000 tape hours.

MountainGate has also informed Convex that drives serviced with regular Preventive Maintenance (PMs), the 50 hour PM and 1000 hr PM, demonstrate a higher reliability than drives without these PMs. Please perform the scheduled PMs to maintain the drive reliability.

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6.44.3 Important Metrum (now MountainGate) Field Issues!(continued)

Item 2: Media compatibility (M120 and T180 tapes)

Due to a head contouring effect with different media types (M120 and T180 tapes), MountainGate does not recommend mixing media types. Unfortunately, we implicitly do this with our field sparing model since we only have one type of tape drive which can go to either a M120 site or a T180 site.

Currently, RSP2150 drives are being contoured for M120 tapes. If you have a customer with T180 tapes and experience problems (read and write errors), please return the drive. The T180 tapes should work in a M120 contoured drive. Internally to the drive and not visible at the application level, there will be a higher correctable bit error rate.

We have found some drives where T180 tapes did fail and have asked MountainGate to implement testing of M120 and T180 tapes before they ship the drives to Convex. Convex will audit this process by doing our own testing to ensure this mixed-media testing is being implemented at MountainGate.

Here is the statement from MountainGate:

"Metrum's Report 'RSP-2150 Tape Evaluations' states that each type of tape contours the heads with a different radius. Using T180 tapes on a unit which has the heads contoured to the T120 tape radius will cause a degraded raw bit error rate, which in this case, corresponds to approximately 1 magnitude difference in the un-collected bit error rate. A total of 20-40 hours of head contact time are required to fully contour a head to a single tape type. Metrum recommends the use of one type of tape for maximum reliability."

(I think the "un-collected" should be "uncorrectable").

Remember, Convex only supports the T120 and T180 tape types and not the T160.

Item 3: Field Manuals

We are in the process of having MountainGate update various manuals to fix errors and to reduce some vagueness in alignment and install procedures. If you have any input on changes, please let Kelvyn know. Secondly, we need a count of who would like new manuals. They probably won't be ready until after the first of the year. Included in the manuals will be a torque spec for the bezel screws, changes to accurately reflect switch and LED settings, and a more scientific approach to aligning drives in a robot.

Item 4: Maintenance cost

Convex's maintenance costs will be increasing for the RSP2150 drives to accurately reflect our effort in supporting these drives. Steve Strachan will provide more information on this item.

Item 5: Other general items

We are working with MountainGate on the next revision of firmware, V6.xx. Currently, there are problems with the current beta firmware V6.02 and we will not release this to the field. Most likely, we will not have a revision released until next year.

FIELD SUPPORT TECHNICAL BULLETIN

Volume: 6 Week: 45 Page: 1 of 1

Contents of this issue:

1. Release of FMI-112 and FMI-113

6.45.1 Release of FMI-112 and FMI-113

FMI0112 and FMI0113 have been released. Copies of these FMI's will be sent to each field office in the next week.

FMI0112

Title: SPP1200 ASB 410-001455-200 Assy. Rev. D or E to Assy. Rev. F
ASB 410-002455-200 Assy. Rev. B or C to Assy. Rev. D

Purpose of Change:
Remove 2 bypass capacitors which may interfere with or cause damage to the -2 VTT and -1.2 SCI (Booster) power bricks.

Priority:
Rework ASB's in the field, when a suspected +1.2 SCI, -2 VTT or VCCMU failure occurs.

FMI0113

Title: Differential to Single Ended Converter Mounting Modification

Purpose of Change:
Prevent damage to a component on some Differential to Single Ended Converters in SPP Differential I/O Chassis'.

Priority:
Install on next P.M.

FIELD SUPPORT TECHNICAL BULLETIN

Volume: 6 Week: 47 Page: 1 of 1

Contents of this issue:
1. SPP 1000/1200 Teststation DAT

6.47.1 SPP 1000/1200 Teststation DAT

Several months ago the DAT drive, on the teststation, was replced with the 217-000012-010. This drive incorporates a Media Recognition switch, sw3, do ensure the proper tapes are used for backups.

There are two types of tapes. Standard video quality DAT tape and DDS tape. DDS tape is a much higher quality. HP had reports of lost, or partial loses of backups with standard quality tapes. Therefore they implemented the MRS, Media Recognition System, to ensure that a DDS quality tape is used when writing.

All of these drives have been shipped with sw 3 in the off position, which will prevent writes to standard DAT tapes. If it is necessary to write to a stand video quality tape, then this switch can be moved to the on position.

If this is done, then the customer assumes responsibility for any lost data.

used when writing.

FIELD SUPPORT TECHNICAL BULLETIN

Volume: 6 Week: 48 Page: 1 of 2

Contents of this issue:

1. MTV Removal Warning for SPP1000/1200's
2. FM0114 SIOP2 (410-006376-200 and 410-007376-200) Assembly Rev. B to C

6.48.1 MTV Removal Warning for SPP1000/1200's

NOTE: This Bulletin Supersedes Bulletin 6.41.1

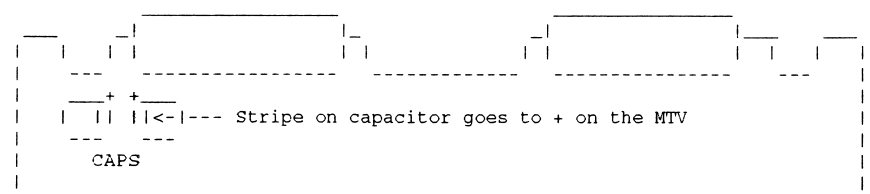
Capacitors exist on the solder side of the wire rev B MTV's, which are required for noise reduction. Without these caps, the MTV's will be susceptible to intermittent and random single and double bit ECC errors.

This is important to understand, because in the 0, or bottom position, it is very easy to knock these caps off, due to poor clearance on a single pem nut, on the right hand bottom side of the node.

This damage can be avoided by ensuring that upward pressure is maintained on the MTV during the entire removal process. This will allow the caps, on the connector side of the board, to easily clear this obstacle, when removed.

Because the damage can be so subtle and thus go unnoticed, it is recommended that all wire rev B MTV's be inspected. If one of the caps is found missing, it may be possible to replace the missing cap(s) in the field. The cap part number is 111-000004-001. These caps are polarized so care should be taken to attach the end of the cap with the stripe to the pad marked with a +. If it is not possible to replace a missing cap, a replacement MTV should be ordered.

EXAMPLE



SOLDER SIDE

NOTE Caps would be on opposite side, from this when installed in system, as MTV is installed component side up.

To verify rev B boards, the cop can be utilized. The wire rev is listed under the "wr" header.

Although the damage will only occur on MTV's in slice 0, it is recommended that all boards be checked, as memory boards may have been rotated within the system.

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6.48.2 FM0114 SIOP2 (410-006376-200 and 410-007376-200) Assembly Rev. B to C

FM0114 has been released. Copies of this FMI will be sent to each field office within the next 2 weeks.

This FMI only effects 3 systems: 65541, 65643 and 65662.
A copy of this FMI and the required part will be shipped to the field location maintaining the system as soon as they are available.

Purpose of Change:

Scanning a SPP1200 can cause components on a SIOP2 (410-006376-200 or 410-007376-200)Assembly Revision B to burn.

Priority:

Problem represents a possible safety hazard.
Implement immediately.

FIELD SUPPORT TECHNICAL BULLETIN

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Contents of this issue:

1. New SPP FDDI Controller
2. SPP DAT Drives Require MRS Tapes
3. MU Bus Errors on SPP1000/1200 CD's

6.49.1 New SPP FDDI Controller

There is a new FDDI controller for the SPP1000/1200.
The part number is 220-000046-201.

This controller WILL NOT work with any SPP-UX release below 3.0.5.

This should not cause any problems, in the field, as SPP-UX 3.1 has been released and is mandatory for all SPP1000/1200 systems.

As old FDDI controllers (220-000046-200) fail and are returned for repair, they will be upgraded to 220-000046-201's.

6.49.2 SPP DAT Drives Require MRS Tapes

As DAT drive capacities increase, manufacturers are requiring MRS (Media Recognition System) tapes be used. Use of non-MRS tapes jeopardizes data integrity.

MRS tapes can be identified by the "MRS" label printed on each tape.

Use of non-MRS tapes will result in errors ,during write operations,that look similar to this:

```
+++> 302
<Tue Nov 28 09:12:01 1995>  warning:0x72000001
<OS>:0.0.0.0:<src ref>:2579528
node: 0x0 (0)
[CC 0x72000001 SR 0x275c48] scsi tape(0:1:0:0,DAT:0 write(0xa) Data Protect
ASC= 0x30 ASCQ=0x0
****
```

FIELD SUPPORT TECHNICAL BULLETIN

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6.49.3 MU Bus Errors on SPP1000/1200 CD's

The current firmware release has a bug in the MU firmware, which under certain circumstances, will produce the following error, on the LCD display:

```
LCD-Display:    BERR        00F5D0D4
                Source      00000005
                PC          00FE36B8
```

This bug usually occurs after a ssystem crash and while performing some debug procedure, such as a crashdump, or a dump_all. It is also possible to encounter this during a reboot. The fault is generally cleared with a do_reset.

This bug will be corrected in the next firmware release.

Again, this problem has been seen on CD's only.